Office of
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Advanced Manufacturing Office

Workshop on Ultra-Precision Control for Ultra-Efficient Devices

Workshop Report

April 21-23, 2021

Within the DOE Office of Energy Efficiency and Renewable Energy (EERE), the Advanced Manufacturing Office (AMO) collaborates with industry, small business, universities, national laboratories, state and local governments, and other stakeholders on emerging manufacturing technologies to drive U.S. industrial decarbonization, economic competitiveness, and energy productivity. AMO has a mission to develop technologies that reduce manufacturing energy intensity and industrial carbon emissions; increase the competitiveness of the U.S. manufacturing sector, with a focus on clean energy manufacturing; and reduce the life cycle energy and carbon impact of manufactured goods in the industry, buildings, transport, power, and agricultural sectors.

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List of Acronyms

AFM	Atomic force microscopy
AI/ML	Artificial intelligence/machine learning
ALD	Atomic layer deposition
ALE	Atomic layer etching
AMO	Advanced Manufacturing Office
APAM	Atomically precise advanced manufacturing
ASD	Area selective deposition
BEETS	Big Energy Efficient Transistor
BJT	Bipolar junction transistor—non-CMOS
CD-SAXS	Critical dimension small-angle X-ray scattering
CD-SEM	Critical dimension scanning electron microscopy
CMOS	Complementary metal-oxide semiconductor
CNT	Carbon nanotube
CRS	Congressional Research Service
CVD	Chemical vapor deposition
DOE	Department of Energy
ECRAM	Electrochemical random-access memory
EERE	Office of Energy Efficiency and Renewable Energy
EUV	Extreme ultraviolet
FeFET	Ferroelectric field effect transistor
FET	Field effect transistor—used in CMOS
FEOL	Front-end-of-line
FeRAM	Ferroelectric random-access memory

FIB	Focused ion beam
GHG	Greenhouse gas
HDL	Hydrogen de-passivation lithography
IC	Integrated circuit
ICT	Information and communication technology
IoT	Internet of things
IP	Intellectual property
IV	Current-voltage
ME	Magnetoelectric
MEMS	Micro-electromechanical system
MESO	Magnetoelectric spin-orbit
MIM	Microwave impedance microscopy
MMIC	Monolithic microwave integrated circuit
MOSFET	Metal oxide semiconductor field effect transistor
MRAM	Magnetoresistive random access memory
NIST	National Institute of Standards and Technology
NSF	National Science Foundation
PCM	Phase change memory
PPACT	Power, performance, area, cost, and time
R&D	Research and development
RDD&D	Research, development, demonstration, and deployment
RF	Radio frequency
ROI	Return-on-investment
RRAM	Resistive random-access memory

SAXS	Small angle X-ray scattering
SBIR/STTR	Small business innovation research/small business technology transfer
SC	Office of Science
SEM	Scanning electron microscopy
SI	International System of Units
SIA	Semiconductor Industry Association
SOI	Silicon-on-insulator
SOT	Spin orbit torque
SPM	Scanning probe microscopy
SRC	Semiconductor Research Corporation
STEM	Scanning transmission electron microscopy
STM	Scanning tunneling microscopy
STT	Spin transfer torque
TEM	Transmission electron microscopy
TFET	Tunneling field-effect transistor
UPM	Ultra-precise manufacturing
VLSI	Very large-scale integration
XRD	X-ray diffraction
XRF	X-ray fluorescence
XRR	X-ray reflectometry

Executive Summary

The U.S. Department of Energy's (DOE's) Advanced Manufacturing Office (AMO) held its second virtual Workshop on Semiconductor R&D for Energy Efficiency on April 21–23, 2021. This public workshop—titled Ultra Precision Control for Ultra Efficient Devices—brought together more than 200 leading scientific and technical experts to identify opportunities to use ultra-precise manufacturing (UPM) processes and metrology and characterization tools to accelerate the development and deployment of ultra-energy-efficient devices. The workshop featured perspectives of researchers from national laboratories, universities, government agencies, and industry with expertise in devices, processes, and metrology and characterization. This workshop was intended to inform an AMO research, development, demonstration and deployment (RDD&D) plan to significantly reduce semiconductor energy use by 2030.[1]

The initial plenary and panel speakers clarified the strong alignment of AMO's, the office of Energy Efficiency and Renewable Energy's (EERE's), DOE's, and the federal government's RDD&D goals with the goals of the semiconductor industry. The semiconductor chip shortage—especially for the automotive industry—was also noted as a sign of the need for more investment in U.S. semiconductor manufacturing. After the introductory plenaries, the workshop was divided into three technical topics: ultra-energy-efficient devices, UPM processes, and UPM tools and characterization. Each technical topic included a moderated panel discussion and a facilitated session.

The following themes were emphasized during the workshop discussions:

- The need for ultra-energy-efficient semiconductor devices and processes in the next decade.
- The potential to accelerate the growth of the domestic high-tech workforce through RDD&D investments in the semiconductor industry.
- The importance of RDD&D investments in the following priority research areas, for the development of ultra-energy efficient semiconductor devices:
    - Co-design
    - Processes
    - Materials
    - Chemistry
    - Metrology.

The highly interrelated nature of the workshop's three technical topics is apparent when comparing the priority research areas and their relationship to these technical topics, shown in Table ES-1. Five of the six priority research areas, described below, are directly relevant to two or more of the technical topics.

1. **Co-design: extending energy-efficiency beyond the device level**: Although device-level improvements are necessary for large gains in energy efficiency or other performance metrics, device-level improvements may not be sufficient to translate into increases in system-level efficiency when fully integrated. A co-design approach is necessary to ensure and maximize system-level efficiency by improving understanding of the relationship between system-level and device-level performance. Co-design is also an effective means to focus resources on innovative concepts that have the best system-level performance potential. Collaboration between researchers at different levels of the stack and those in a variety of fields will provide the diverse knowledge base needed to tackle this problem.

[1] This workshop report summarizes the presentations, panel discussions, and facilitated discussions that took place at this event. More detailed summaries are available in the Appendix. Note that the results presented here are a snapshot of the viewpoints expressed by the experts who attended the workshop and do not necessarily reflect those of the broader device, semiconductor manufacturing, and metrology and characterization communities.

2. **Processes: establishing a partnership-based approach to introducing ultra-precision processes**: The increasing complexity of emerging ultra-efficient devices and interconnect fabrics will require ultra-precision process development to manufacture them. Contributing to this complexity are the increasing heterogeneity of materials combinations, the push towards three dimensional devices, interconnects, and their integration including, the need for ultra-precision in pattern transfer and material interfaces. Workshop participants identified collaboration with toolmakers as an essential step toward successful introduction of ultra-precision manufacturing processes at scale. This collaborative approach could be a win-win scenario where ultra-precision processes benefit the toolmakers by helping to solve their immediate problems (e.g., contact resistance) and in turn, toolmakers benefit the ultra-precision process development by helping ensure that each of the newly developed processes for ultra-efficient devices is compatible with existing manufacturing processes, especially thermal budget and potential contamination issues.

3. **Materials: leveraging atomic precision to engineer conventional materials (rather than using new materials)**: Novel materials or material combinations are necessary in some of the most promising ultra-efficient devices. However, these materials face material growth and material and interfacial quality challenges that have hindered their commercialization. At the same time, contamination of existing process lines from these novel materials makes chip manufacturers hesitant to adopt these technologies. Recent advances in ultra-precision atomic manipulation to engineer materials' electronic properties suggests that some of these novel materials can be replaced with more common ones. Conventional materials have the advantages of avoiding the need for new material growth and synthesis processes and having mature, established supply chains. One critical challenge facing this approach is the severely diminished throughput for producing today's engineered materials compared with conventional growth and synthesis processes.

4. **Chemistry: identifying promising precursors for surface chemistry-based self-assembly approaches**: Many of the most scalable UPM processes that are energy efficient are bottom-up (e.g., self-assembly) approaches that rely on surface chemistry to etch, deposit, or pattern. Optimizing the complex chemical compounds (i.e., precursors) that these processes depend on can greatly enhance reaction kinetics, materials coverage, and process reliability. High throughput experimentation and machine learning (ML) can be leveraged to accelerate the discovery of promising precursors and develop scalable processes to manufacture them. If these processes can be scaled, the aforementioned technologies for engineered materials may also be needed to guide certain self-assembly processes.

5. **Metrology: combining approaches for more energy efficient and secure metrology**: As devices shrink, the number and importance of metrology steps increases, as does the importance of *decreasing process variability*. In-situ metrology helps researchers and manufacturers better understand sources of variability and better control their processes. Furthermore, most metrology and characterization methods used today rely on a modeling step for parameter estimation and understanding the underlying physics is critical to truly comprehend and make use of the measurements. Hybrid metrology, a technique where multiple tools are used, is able to further reduce uncertainties compared with model-based measurements alone. AI/ML can be leveraged with the influx of data from metrology steps to drastically reduce the data stored and transmitted and improve the energy efficiency and security of these metrology steps.

Throughout the workshop, a number of cross-cutting issues emerged. These are topics that are not strictly research focused but are included because they continued to come up in all research needs discussions. The most prevalent was limited access to facilities and equipment for academic and small business researchers, summarized below.

Access to facilities and equipment: Improving access to state-of-the-art facilities and equipment was stressed multiple times throughout the workshop. During the federal panel Q&A, Lloyd Whitman from the National Science Foundation (NSF) noted this is a significant need for academic researchers as highlighted by a recent workshop on the topic (Basu et al. 2021). In addition to academic researchers, participants noted that small business researchers also cannot access equipment at large foundries due to economics, material contamination concerns, and schedule. In addition, advanced node foundries do not currently exist in the United States. Industry-government partnerships to build and enable access to state-of-the-art semiconductor fabrication capabilities for prototyping new devices and circuit designs will accelerate progress on new device commercialization.

Table ES-1: A crosswalk between priority research areas and technical topics

Priority research area	Workshop Technical Topic		
	Devices	Processes	Metrology and Tools
Co-design	X	X	X
Processes	X	X	X
Materials	X	X	X
Chemistry		X	
Metrology		X	X
Access to facilities and equipment	X	X	X

Based on report outs and discussions on the workshop's final day the following **takeaways** emerged:

- For emerging devices, industry must be guided by a holistic set of metrics, not just energy efficiency, because customers will expect energy efficiency while also improving or at least maintaining other performance metrics of today's devices.
- The capital cost and energy consumption of semiconductor manufacturing is very high and growing rapidly.
- Development of emerging energy-efficient devices can drive the growth of U.S. semiconductor manufacturing (now 12%) to a leadership level (35%–40%).
- The domestic semiconductor industry workforce must grow if the United States is to take a leading role in semiconductor manufacturing.
- Improvements in the manufacturability of ultra-energy-efficient technologies can increase U.S. semiconductor manufacturing and the number of well-paying jobs.
- Digitalization of manufacturing (Industry 4.0) will drive a growing need for more semiconductor devices and products.
- Innovation in semiconductor manufacturing will help reach the Biden Administration's climate and energy goals (e.g., net-zero greenhouse gas emissions by 2050).
- Manufacturers will need to increase their use of semiconductors to finely control their processes as they pursue electrification for decarbonization.
- Ultra-energy-efficient technologies will enable the continued growth of our world economy without a corresponding increase in planetary energy use.
- AMO investments in UPM for transistor, memories, interconnects, and 3D integration technologies are promising and could decrease transistor use by a factor of 10.
- The U.S. manufacturing sector is more supportive of a U.S. semiconductor supply chain to prevent chip shortages that are currently slowing automotive and other manufacturing.

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Background

On April 21–23, the U.S. Department of Energy's (DOE's) Advanced Manufacturing Office (AMO) within the office of Energy Efficiency and Renewable Energy (EERE) held the second in a series of workshops on different topics related to semiconductor research and development (R&D) to increase energy efficiency. This workshop focused on ultra-energy-efficient devices and the ultra-precision manufacturing (UPM) processes and next-generation control and metrology technologies needed to manufacture these devices. In addition to the industry needs and RDD&D opportunities, AMO's new goal on greenhouse gas (GHG) reduction was addressed. The output of this workshop will inform AMO's future R&D portfolio investments; provide perspectives on trends, drivers, and challenges for ultra-energy-efficient devices and enabling technologies; and help the stakeholder community understand the opportunities on the horizon.

The work that you're doing to develop ultra-precise manufacturing technologies will help increase the competitiveness of domestic semiconductor manufacturing, spur domestic job creation, and combat the climate crisis through reduced energy consumption across all sectors that use semiconductor technology.

– Kelly Speakes-Backman,
Acting Assistant Secretary, EERE

Workshop Series

Semiconductors power key products that are rapidly growing in importance in all sectors of the economy, including consumer goods, finance, transportation, and manufacturing. Advances in semiconductor technology are critical for global competitiveness as well as economic, national, and climate security. According to an October 2020 Congressional Research Service (CRS) report, the global semiconductor industry in 2019 had $424 billion in sales with the United States accounting for roughly half. The CRS divides the industry into four segments, shown in Figure 1. Because of its economic importance and the potential for its products to improve quality of life and reduce energy use in other sectors, growth of the semiconductor industry is desired; but innovation is needed to ensure this growth is accompanied by major improvements in energy efficiency. In the past, semiconductor industry and product energy use were flat or declining due to efficiency innovations. However, since 2010, as shown in Figure 2, it has begun to dramatically increase--doubling every 3 years (SIA 2019).

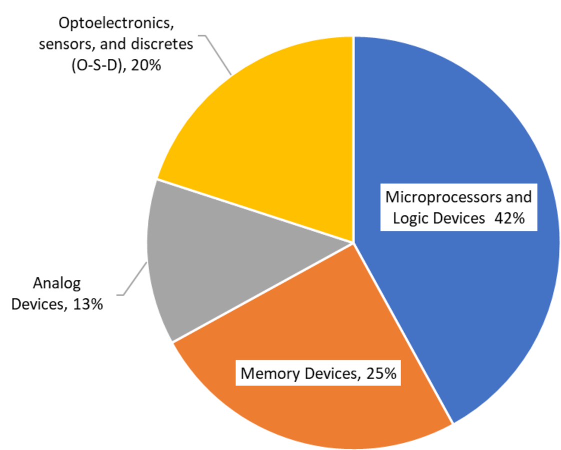

Figure 1: Market segments of the semiconductor industry and the breakdown of sales, in percentages. Logic, memory, and RF devices, one of the primary subjects of the workshop, represent roughly 80% of the semiconductor market, equating to approximately $340 billion in sales.

Multiple trends in semiconductor related energy use are combining to make increased energy efficiency a top priority for the industry and the federal government.

These trends include the increasing energy consumption of semiconductor manufacturing processes; the decrease in improvements in energy consumption per chip; and the acceleration of the use of microelectronics in products and processes—which, ultimately, has substantially increased the overall energy use of semiconductor industry processes and products.

A major new driver for AMO efforts with respect to semiconductor energy efficiency is the Biden Administration's goal of cutting GHG emissions by 50% by 2030 through aggressive industrial decarbonization and electrification. This has led to an increased EERE interest in developing more energy efficient semiconductor devices. U.S. leadership in manufacturing and deploying these devices can lead to a reshoring of semiconductor manufacturing foundries spurring domestic job creation, increasing productivity and competitiveness of the U.S. manufacturing industry, and combatting the climate crisis through reduced energy consumption across all sectors that utilize semiconductor technology. Other Biden Administration carbon goals that drive semiconductor efficiency R&D include goals for a zero-carbon grid by 2035 and the overall goal of a net zero carbon economy by 2050. These goals all increase the urgency of deploying decarbonization technologies such as extreme energy efficiency, massive electrification, and increased digitalization that increase use of semiconductors.

From her first day in office, Secretary Granholm has emphasized DOE's role to make scientific breakthroughs, turn them into technologies, and deploy the technologies in a way that creates good-paying jobs, ensures racial justice, and encourages collaboration. AMO's Assistant Secretary repeated these themes when she gave a keynote talk at this workshop where she discussed flattening the curve of semiconductor energy use to addressing the climate crisis. She also talked about the potential for increasing good-paying jobs by bringing semiconductor manufacturing back to the United States, the need for encouraging collaboration across the government, and the need to involve disadvantaged communities.

Workshop Motivation

Semiconductor industry products power nearly every aspect of our lives, and their use is expected to continue to grow exponentially with the rapid digitalization of our modern economy in a post-pandemic world. Large industries such as telecommunications, the Internet of Things (IoT), and manufacturing are integrating more and more advanced semiconductor products into their products and processes. At the same time, Moore's Law efficiency increases due to device miniaturization have reached their physical limits. Due to these trends, semiconductor energy use is on track to become a major fraction of planetary energy use. As shown in Figure 2, computational energy use has doubled nearly every three years since 2010 (SRC 2021) and the doubling time may continue to shorten. For example, semiconductor energy use is already the dominant source of carbon emissions for research itself in major areas supported by DOE (Feder 2021). Specific semiconductor technology applications (e.g., bitcoin mining [2], artificial intelligence[3]) show even faster doubling times so that energy use from semiconductors could become a major source of GHG pollution before the electricity grid reaches net zero carbon emissions. Without significant investments in energy efficiency for semiconductors, they could add another 20% to electricity demand by 2035 (SRC 2021). Ultra-energy-efficient semiconductor devices and architectures commercialized before 2030 could help curb this unsustainable use of electricity.

[2] A *New York Times* analysis (Huang, 2021) showed that bitcoin mining energy use is now doubling every year
[3] Mehonic and Kenyon, 2021, shows leading artificial intelligence programs doubling energy use every 2 months.

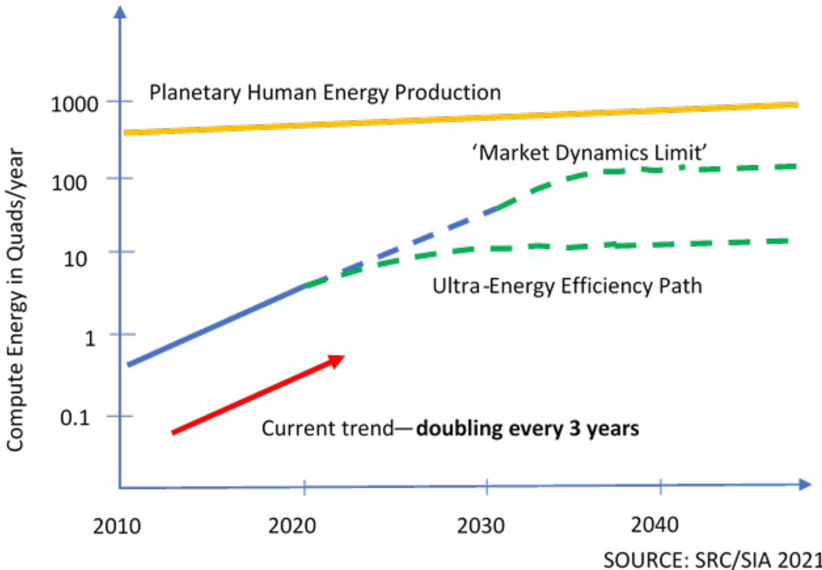

Figure 2: At current growth rates of computational energy use, the "Market Dynamics Limit" will be reached by 2035, limiting the world's computing capacity and economic growth. Alternatively, prioritizing ultra-high energy efficiency in semiconductor products can achieve an 'ultra-energy-efficiency' trajectory in which computing/economic growth and energy use are decoupled.

Figure 2 shows that ultra-energy-efficient devices and the end-use products into which they are incorporated must be drastically more energy efficient ("ultra-energy-efficiency path") to flatten the curve of semiconductor energy use. UPM processes, tools, and metrology will provide the necessary manufacturing innovations necessary to enable these ultra-efficient devices. Addressing challenges and exploring opportunities in these separate but interconnected topics can provide the best path forward to drastically reduce semiconductor energy use.

The looming semiconductor energy impact also comes at a time when the Biden-Harris Administration is accelerating the U.S. response to the climate crisis. The nation is at an inflection point where federal investment in joint R&D for semiconductors—including the underlying manufacturing technologies for the next generation of devices—could accelerate our transition toward a sustainable path that avoids planetary energy impacts, while revitalizing a key domestic industry that offers high-paying jobs.

By partnering with U.S. industry to further develop UPM technologies, AMO hopes to increase the competitiveness of domestic device and chip manufacturing, spur domestic job creation in this growing field, and combat the climate crisis by flattening the curve of semiconductor energy consumption across all sectors that use semiconductors by 2030.

AMO began its atomically precise manufacturing program in 2015 based on the hypothesis that increasing control at the atomic scale yields greater energy efficiency. As manufacturing technology has become more advanced, manufacturing precision has similarly developed, from the millimeter scale to the sub-nanometer scale. Projects within the program address critical needs in devices, UPM processes, and UPM tools, the three technical topics of the workshop. The workshop aimed to identify emerging ultra-energy-efficient devices and UPM processes and tools, critical challenges, and key R&D opportunities to further expand and grow AMO's semiconductor R&D efforts with particular focus on energy efficiency.

Workshop Overview

To better understand the challenges and opportunities in developing ultra-energy-efficient devices and their enabling manufacturing and metrology technologies and AMO's role in this area, DOE held the Workshop on

Ultra Precision Control for Ultra-efficient Devices on April 21–23, 2021. Representatives from industry, academia, the DOE national laboratories, and non-governmental organizations gathered virtually to hear presentations and participate in panel discussions with subject matter experts, as well as contribute to topical facilitated discussions/brainstorming sessions. The workshop was divided between three technical topics: ultra-efficient devices, UPM processes, and UPM tools and metrology. This workshop report summarizes the attendees' input on the emerging technologies and RDD&D challenges and opportunities for the three technical workshop topics from the presentations, panels, and facilitated discussions.

Below is a brief overview of the workshop agenda. More detailed summaries of all of the talks are included in Appendix B.

On the first day of the workshop, participants learned about the growing semiconductor energy crisis, the emerging semiconductor devices that will help address this problem, and the Biden Administration and U.S. industry priorities that such research would support. Plenary talks featured speakers from DOE and the Semiconductor Research Corporation (SRC). The first panel session included representatives from different government agencies on their semiconductor R&D efforts broadly. Next, a keynote from SRC focused on prospects for energy efficiency and paths forward to address the growing semiconductor energy crisis. The day concluded with a panel and facilitated discussion on ultra-energy-efficient devices.

The second day began with an interactive talk about the motivation for dividing the workshop into devices, processes, and metrology as well as a discussion of another recent workshop focused on atomic precision. The workshop then moved onto panel discussions. The first focused on UPM processes and included a talk from one of AMO's current projects followed by extensive Q&A. The next panel focused on UPM tools and metrology and also included a talk from an AMO sponsored project. Both panel sessions were followed by a facilitated discussion.

The third and final day summarized the findings of Day 1 and Day 2 with an extensive report-out session covering the three technical topics and a discussion on priority research directions. The workshop concluded with a talk discussing historical and future trends of computing and other elements (e.g., architecture) needed to achieve sustainable computing.

Each of the workshop sessions, including the three technical topics, are summarized below.

Opening Plenary Session

The opening plenary and panel speakers clarified the strong alignment of AMO, EERE, DOE, and the federal government's RDD&D goals with the goals of the semiconductor industry. For example, on Day 1, Tina Kaarsberg, chair of the workshop series, noted that AMO's second goal for increased lifecycle and materials efficiency of manufactured products is supported by numerous specific goals in SRC's decadal plan, especially its fifth grand goal to discover computing paradigms/architectures with a radically new computing trajectory, demonstrating >1,000,000x improvement in energy efficiency.

The government keynote speech by EERE's Acting Assistant Secretary, Kelly Speakes-Backman, also strongly emphasized the DOE and semiconductor industry's common cause for increasing energy efficiency and warned that without dramatic improvements in device and computing system efficiency, semiconductors could shift from being a climate solution to a climate problem, as shown in Figure 2. She also noted that investments in manufacturing RDD&D for ultra-energy-efficient semiconductor devices can bolster the domestic semiconductor manufacturing industry by increasing its competitiveness and size, and expanding the well-paid workforce. She noted this was one key reason that the Administration's American Jobs Plan called for $50 billion in semiconductor manufacturing and research at DOE and other agencies.

The industry keynote by SRC Chairman and President Todd Younkin echoed Acting Assistant Secretary Speakes-Backman's remarks about the need for energy efficiency and increased investments in semiconductor manufacturing and workforce. He, and several speakers that followed, also provided numerous examples of research, demonstration, and deployment efforts needed for co-design of new energy efficient systems up and down the stack; advanced metrology; manufacturing R&D for materials and processes; and joint, basic applied research in physics, materials, and chemistry. All plenary speakers and the government panel emphasized the need for industry government partnerships and access to advanced facilities. Details on these presentations can be found in the speaker summaries in Appendix B. Multiple plenary and panel speakers emphasized the following themes:

- The need for semiconductor ultra-energy efficiency in a decade.
- The potential to accelerate the growth of the domestic high-tech workforce through RDD&D investments in the semiconductor industry.
- The importance of RDD&D investments in the following priority research areas, for the development of ultra-energy-efficient semiconductor devices:
  - Co-design
  - Processes
  - Materials
  - Chemistry
  - Metrology.

After the plenary talks and the Federal Panel summarizing the federal semiconductor R&D ecosystem, came the panel session and facilitated discussion for each of the technical topics, Ultra-efficient Devices, Ultra Precise Manufacturing Processes, and Ultra Precise Manufacturing Tools and Metrology. Each are summarized below. This report also includes a fourth section, Cross Cutting Issues, that summarizes the cross-cutting topics that were identified across the three technical topics.

Ultra-Energy-Efficient Devices

The metal-oxide-semiconductor field-effect transistor (MOSFET)—the basis for today's logic, memory, and radio frequency (RF) device architectures—is reaching its fundamental thermodynamic limit for switching. MOSFETs' diminishing improvements in energy efficiency can no longer offset the energy consumption associated with their exponentially increasing use. As detailed in the read-ahead document, many new devices utilizing new materials (including engineered materials) and device physics that can exceed current MOSFET-based devices in energy efficiency are being explored. AMO is most interested in those that have the potential to be commercialized by 2030. As a result, the Device panel's presentations and discussions were focused on those with potential to be integrated with today's complementary metal-oxide semiconductor (CMOS) fabrication lines.

The Devices session began with a plenary talk by Victor Zhirnov, chief scientist of SRC, discussing the current trajectory of computational energy use and the thermodynamic parameters that need to increase to reduce energy consumption by orders of magnitude. He also discussed how the energy consumption of device types had changed over time, Figure 3. A panel session focusing on emerging ultra-efficient logic, memory, and RF/communications devices that could be commercial by 2030 followed. Note that the categories of devices are not mutually exclusive.

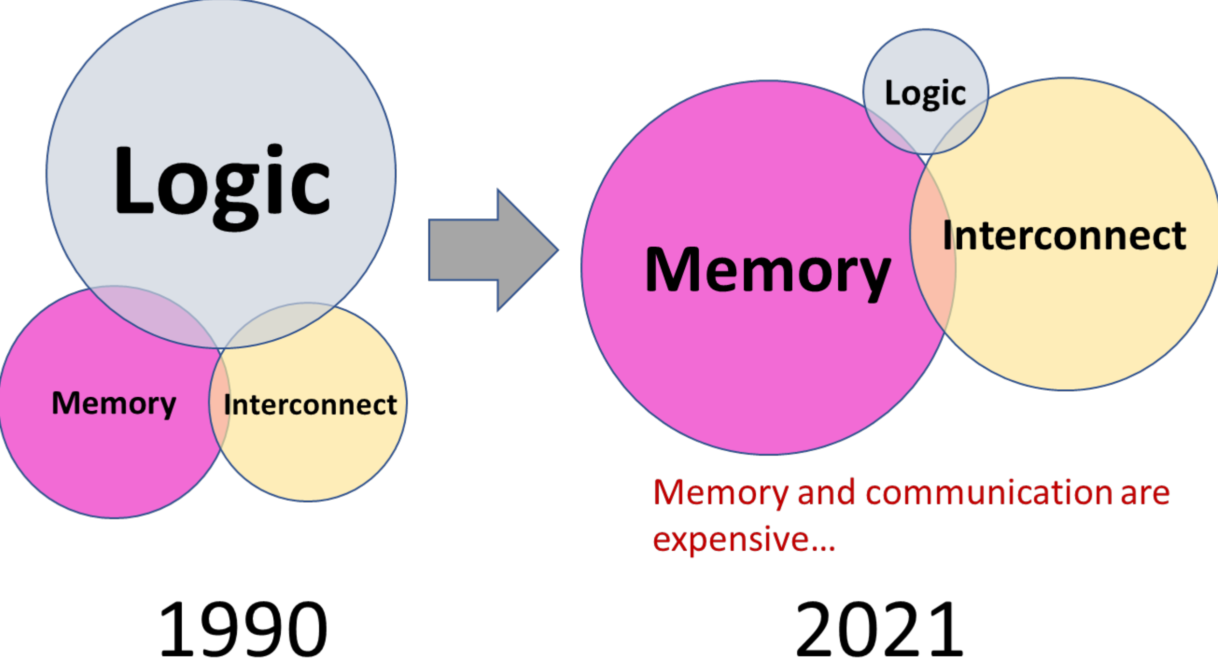

Figure 3: Relative energy consumption of logic, memory, and interconnects in 1990 and 2021. With Moore's Law and other improvements—such as new materials and device architectures—primarily directed at logic devices, energy consumption of memory and interconnects outpaced that of logic. Source: Zhirnov, V., 2021

Panelist Alan Seabaugh (University of Notre Dame) discussed the pros and cons of two promising, ultra-efficient logic devices, tunneling field-effect transistors (TFET) and ferroelectric field-effect transistors (FeFET); Dmitri Nikonov (Intel) discussed the magnetoelectric spin-orbit (MESO) as a logic device; Carlos H. Diaz (TSMC) provided an overview of promising, ultra-efficient memory devices and the critical parameters of interest; and finally, David Howard discussed TowerJazz's history and capabilities in RF electronics. A vigorous Q&A session followed the panel talks. Key concepts and takeaways discussed during the Devices plenary talk, panel session, and facilitated discussions are discussed in the following sections. A more detailed summary of the plenary talk and each panel speakers can be found in Appendix B. Table 1, at the end of the Devices chapter summarizes participant input from the facilitated session identifying the most common device parameters that may suffer when maximizing for energy efficiency and R&D challenges and opportunity areas. Table C-1 to Table C-3 includes the full participant input.

Near-term Emerging Ultra-energy-efficient Devices

As shown in Figure 1, device markets are generally divided according to their function. Underlying these functions in the near term are three primary device types: logic, memory, and RF.

Ultra-energy-efficient Logic Devices

AMO is already conducting ultra-precision manufacturing research supporting 7 of the top 14 logic devices identified in the International Roadmap for Devices and Systems (IRDS): 2020 Edition. Emerging logic devices can be conceptually divided according to their switching mechanism: electric charge, magnetism/spin, or other "state variables."[4] Several new devices, however, use more than one mechanism. According to the IRDS (2020), these logic device challenges include the need for:

- Full interface control and a bandgap (e.g., TFETs, graphene).
- Synthesis (e.g., carbon nanotubes [CNTs]) with tight distribution of bandgap and mobility.
- Low defect density (e.g., complex metal oxides).
- Low-resistance ohmic contacts (e.g., high-mobility transition metal dichalcogenides).

Summarized below are logic devices with improved energy efficiency that were discussed during the workshop:

Tunnel Field-Effect Transistors (TFET): Transistors based on quantum tunneling rather than thermionic emission have been shown to operate at 1/10 the power of leading-edge conventional transistors (MOSFET) (with switching energy as low as $2x10^{-18}$ Joules, or 2 attojoules). TFET's low subthreshold swing (SS) of less than 60 mV/decade enables lower system power. TFETs' requirement for atomic precision, due to quantum tunneling that is exponentially dependent on the tunnel barrier thickness, is a scale-up challenge. As shown in Figure 4, TFET's current has been too low at higher voltages to serve as a drop-in replacement for conventional CMOS. Fabrication requirements (e.g., high temperature) for atomic precision prevent ready integration of TFET into CMOS, but manufacturing research (described in the next section) is underway to overcome these challenges.

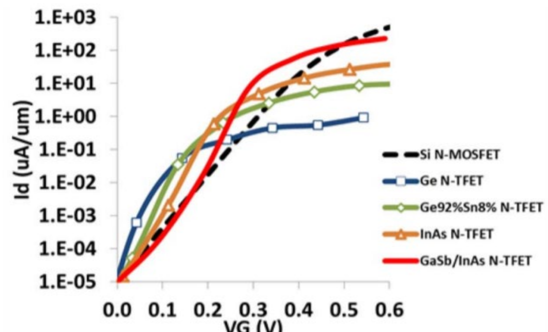

Figure 4: All TFETs exceed the 60 mV/decade upper limit slope of MOSFET (Avci, Morris, and Young 2015).

Spin-Based Logic: MESO devices combine magnetization and polarization in one switch and have the potential to achieve attojoule-class logic gates for computing. MESO logic has collective switching, strong thresholding behavior, and nonvolatility (Manipatruni, Nikonov, and Young 2018). The optimal combination of these two variables keeps the operating voltage, and hence the energy consumption of the device, low. Although these devices are slower than traditional logic devices, speed may not be important when a small energy footprint is desired. However, the wide array of novel materials and layering schemes needed for MESO devices could present manufacturing challenges.

Summarized below are two additional devices that weren't discussed during the workshop but show potential to drastically reduce energy consumption of logic devices.

Carbon Nanomaterials: CNTs' switching energy can be as low as 100 attojoules, two orders of magnitude lower than that of state-of-the-art transistors. But growing defect-free aligned CNTs require atomic-level control. Graphene was the first 2D material used for transistors but its lack of bandgap limits its utility for digital.

[4] State variables refer to the carrier for logic operations.

2D Channel FET: Non-carbon 2D materials, such as transition metal dichalcogenides, are proving to be more promising candidates than graphene for low-energy switching for future devices, as non-carbon materials provide improved electrostatic control and carrier mobility in some materials (Lu and Seabaugh, 2014; Hartmann et al. 2021). Advances in selective atomic layer deposition (ALD), atomic layer etching (ALE), area-selective deposition (ASD) are needed to accelerate commercialization.

Ultra-energy-efficient Memory Devices

As with logic devices, novel channel materials or device physics can be leveraged for ultra-energy-efficient memory devices. AMO's ultra-precision manufacturing R&D portfolio supports four of the top nine memory devices identified in the IRDS. As with logic devices, there are charge- and non-charge-based devices. AMO determined from literature searches where comparative data are available that FeFET and phase change memory (PCM) are among the most promising memory technologies for improved energy efficiency. Spin transfer torque (STT) and ferroelectric random-access memory (FeRAM) devices, two ultra-energy-efficient memory devices, have already been commercialized.[5] According to the IRDS (2020), long-term challenges for these memory devices include:

- Control of oxygen vacancy formation at metal interfaces and interactions of electrodes with oxygen and vacancies (e.g., complex oxides).
- Needs for long-term reliability of the switching mechanism.
- Improvements in switching speed and cyclic endurance.
- Uniformity of the switching bias voltage and resistance, both for the on state and the off state (e.g., conductive bridge RAM, PCM).

FeFET, the most energy-efficient memory device, requires less than 1 femtojoule (10^{-15}J) per bit, while FeRAM and PCM require 50fJ/bit and 3pJ/bit, respectively. For comparison, traditional magnetoresistive random access memory (MRAM), resistive random-access memory (RRAM), and NAND Flash memories require 2pJ/bit, 50pJ/bit, and 1nJ/bit, respectively. The most energy efficient emerging memory devices discussed during the workshop, which still face significant barriers before commercialization, are summarized below:

FeFET: FeFET incorporates a ferroelectric oxide between the channel and gate electrode. The permanent polarization of the ferroelectric material enables its memory capabilities. The 2011 discovery of advanced CMOS-compatible HfO_2-based ferroelectric devices mean that FeFET made from HfO_2 thin films can be used both as non-volatile memory elements and as logic compute elements (Khan, Keshavarzi, and Datta 2020). Hence, FeFETs are likely to be used for non-traditional, in-memory (e.g., neuromorphic) computing data-flow architectures to enable small, energy-efficient systems needed for edge computing (e.g., IoT). Most of FeFET's low energy use is not due to the device itself (which uses more energy than non-STT spintronics device) but to the close physical proximity of memory and logic in the same FeFET device, which avoids energy-intensive data movement. Current manufacturing challenges include improved interface control of the gate stack and polarization hysteresis.

Phase Change Memory (PCM): PCMs are a type of resistance-based memory. These rely on resistance-based read operation of a passive memory device and have high-speed read/write operation (10 ns), ultra-scalability below 10 nm, and compatibility with state-of-the-art CMOS processes. In particular, PCM utilizes changes in conductance caused by changes in a material's crystal structure (crystalline to amorphous), due to thermal input, to achieve memory function. PCMs that can be switched by non-thermal phase changes are also being investigated. Because of the inability of current to flow in the amorphous state, PCM's have negligible leakage and thus promise ultra-low energy consumption and very long memory retention and stability (Le Gallo and

[5] STT MRAM has entered commercial production under the name Everspin at major foundries across the world.

Sebastian 2020). Integration of non-standard materials into current CMOS process flows will be a key challenge in commercialization efforts.

Ultra-Energy-Efficient Radio Frequency (RF)[6] Devices

RF devices and circuits are widely deployed in telecommunication systems. Unlike emerging logic and memory devices, novel, energy efficient RF devices do not leverage new physical phenomena for switching as their operating parameters are not near fundamental physical limits. Still, many new materials are being explored to increase the performance and decrease the energy use of RF devices. The major opportunity and challenge for improving energy efficiency of telecommunication systems are in the devices found in base stations (i.e., communication towers) including transceivers, power amplifiers, and antennas, where 5G networks will require an estimated quadrupling of power, if the technology is not improved.[7]

Today's technology is based on Gallium Arsenide (GaAs), the material of choice for RF since the 1970s, thanks to its high resistivity. High saturation velocity, carrier mobility, and larger bandgap make GaAs more energy efficient than silicon-based RF components. Its mature product lines at large fabrication facilities still make it the go-to material for large-scale monolithic microwave integrated circuit (MMIC) production (Benson 2017). Unlike emerging logic and memory devices that leverage different state variables, emerging RF devices rely on novel materials such that materials processing and growth constitute the main barriers to their widespread commercialization. Summarized below are two materials for emerging RF devices that were prominently discussed during the workshop.

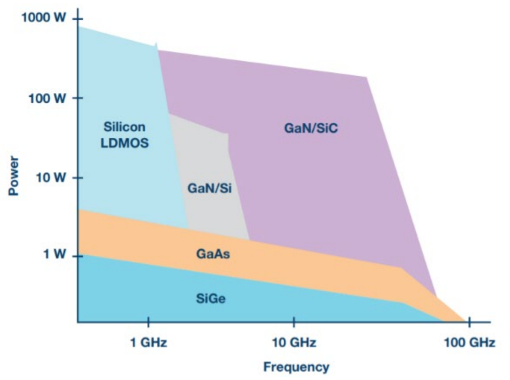

Figure 5: GaN is able to operate at significantly higher power at similar frequencies compared with traditional GaAs and SiGe technology (Benson 2017).

Gallium Nitride: Gallium nitride is an attractive alternative to standard GaAs MMICs because of its higher output power at microwave frequencies and higher operating temperatures and voltages. Faster switching speeds, lower resistance when switching to the "on" state, and higher thermal conductivity make GaN-based RF devices more energy efficient than either GaAs or silicon, Figure 5. Defect-free growth of GaN on native or non-native substrates, however, has proven to be a barrier in transitioning from traditional GaAs or SiGe RF devices to GaN based devices according to workshop attendees.

Carbon Nanotubes (CNTs): CNTs' one-dimensional geometry has inherent linearity, which leads to a high dynamic range. This makes CNT-based devices well suited to electromagnetically noisy environments. In addition, CNT's high carrier mobility, high saturation velocity, and ballistic transport allow for extremely low power operation for CNT circuits. Growing or depositing pristine CNTs with tight diameter control and semiconducting-to-metallic CNT selectivity has presented challenges in fabricating CNT devices at manufacturing-relevant CNT density, current density, and transconductance. Hence CNT device properties still fall short of their theoretical performance values.

[6] Radio frequency devices typically operate between 20 kHz and 300 GHz.

[7] Deploying ultra-energy efficient devices that reduce power consumption in edge devices that rely on wireless communication (e.g., mobile phones, smart watches, and laptops) improve battery life, device lifetime, and mean time to failure, however energy efficiency improvements in these areas are not hitting the same limits of operation as for logic and memory that require enhanced innovation.

Challenges and R&D Opportunities for Ultra-Efficient Devices

There is precedent for energy efficiency to take priority over other performance metrics. As was mentioned during the panel session, this tradeoff was accepted when transitioning from bipolar junction transistors (BJT) to CMOS devices as the primary device in integrated circuits (ICs). Although BJTs exhibited faster switching speeds, CMOS devices ultimately prevailed due to their higher energy efficiency. Industry made a concerted effort to transition to CMOS devices and subsequently developed the necessary infrastructure to support CMOS manufacturing. Similarly, to transition to the aforementioned ultra-energy-efficient technologies, the semiconductor industry again must be aligned and exert a concerted effort towards this change in the coming decade.

However, in developing emerging devices, it is clear that industry must be guided by a holistic set of metrics, not just energy efficiency, and the expectation would be that the non-energy-efficiency performance metrics would be comparable to that of today's devices.

During the Devices session, numerous challenges and R&D opportunities were discussed, summarized below.

Material and interface quality: Semiconductor material quality is critical for proper device functioning. State-of-the-art semiconductor devices now approach atomic scales where materials behave differently than at the bulk scale. Hence references that were historically used in processing, such as material constants and phase-change behavior, have ceased to be applicable. In addition, interfacial quality has become critical, since even a single defect or impurity atom at an interface can drastically alter device performance. Going forward, doping profiles, contacts, and dielectrics will all require pristine interfacial quality—or engineered materials without such interfaces—to achieve theoretical device performance. Atomically precise control has become increasingly important as devices continue to shrink.

Material synthesis: Emerging devices that rely on non-Si materials, such as CNTs, graphene nano-ribbons, other 2D material systems, GaN, etc. often require pristine material growth to achieve theoretical performance targets and to exceed incumbent technology. Consistent, controllable growth that is cost effective is still a challenge to some extent for all non-Si materials. In addition, even processes that show consistent growth at the benchtop scale typically face significant challenges in scale up. Computational fluid dynamics modeling may be a necessity to adequately transition to high volume process chambers typically found in fabs. In addition, development of in-situ characterization was highlighted as a promising path forward in improving synthesis and growth of novel materials. On the other hand, leveraging engineered materials was discussed as an alternative to using non-traditional materials. Advances in atomic manipulation open the door for conventional materials to take on unconventional properties. Not only do these materials avoid novel, complex material growth and synthesis processes, they also have mature, established supply chains.

Material and mechanical stability: Many emerging devices use novel materials that have unknown long term operational stability. Especially in emerging memory devices, cycling may have profound impact on endurance and hysteresis not commonly found in conventional memory devices. As feature sizes decrease, some of these ultra-precise structures may not be robust to the operating currents or voltages of the devices they are intended to replace. In general, novel or non-standard materials may present significant process integration challenges including but not limited to mechanical integrity and thermal stability of the structures and material interfaces, and operational stability issues that may not have been anticipated during early-stage device research. Results presented at the workshop, however, showed that atomically precise structures, such as abrupt doping profiles, proved to be more robust to thermal cycling than conventional CMOS with which they were integrated despite their limited thermal budgets.

Material scarcity: Noble metals have long been the cornerstone for low-contact-resistance materials and their increasing scarcity has become a growing concern. Process materials—those that are not part of the final product, such as hydrofluoric acid and helium—are becoming increasingly scarce as well. In addition,

feedstocks for Si substrates themselves are becoming scarcer as competition for these materials increases, both within the electronics industry and from other industries such as the photovoltaic and display industries.[8]

Contamination: A large number of emerging, ultra-efficient devices rely on novel materials that are not typically found in CMOS fabrication lines. There are significant contamination concerns when introducing new materials into an established fabrication environment. Plasma processing, harsh chemicals, and even air may adsorb chemicals or damage the surface resulting in poor device performance. These materials may adsorb to chamber walls or equipment surfaces and inadvertently deposit on other wafers that use the same tools. These foreign particles may act as mobile ions or charge traps resulting in poor device yield. Although a device may show promise on the R&D level, its adoption at the manufacturing level will require stringent material contamination control to ensure that current process flows are not affected.

Modeling: Modeling of novel devices was stressed to be critically important to understand device performance and its circuit and system level impact. As emerging device rely on atomic-scale interactions, physics-based modeling and understanding of quantum effects and their impact on device performance will be crucial. These quantum effects, coupled with novel material properties, will require the development of new models to predict performance and inform robust circuit designs as well as assess system-level performance benefits of the innovative devices and processes being explored. The development of a multi-scale model that incorporates phenomena at the atomic level to the circuit level with the capability of feeding into traditional design tools was raised as a powerful method in developing next generation devices. AI/ML techniques are useful when plentiful experimental and/or simulation data is available.

Process Development: Process development, especially advances in patterning, was identified as a critical R&D pathway to enable ultra-efficient devices. As emerging devices become more complex in design and material combinations, alignment and pattern-transfer processes will need improved accuracy, precision, and repeatability. Bottom-up fabrication techniques including self-limiting and self-assembling chemical processes were cited as the most scalable approaches to atomic precision, although slower and less scalable techniques may be required to direct the self-assembly process. Area Selective Deposition (ASD) in particular was viewed as a key bottom-up area needing progress.

As was mentioned in the UPM Processes panel session, integration of novel processes or tools in the process flow may require changing several steps prior to and after the step of interest or completely changing a process module. For example, the integration of ALD of high-κ dielectrics not only required changing deposition tools (from chemical vapor deposition (CVD) to ALD) but also required changes in previous steps for surface preparation and changes in steps after deposition. In this way, the manufacture of emerging devices may significantly alter current very large-scale integration (VLSI) processes and facilities.

Understanding Device Failure: Manufacturability of these emerging devices will ultimately decide whether these devices make it past the R&D phase. Evaluating the degradation mechanisms of emerging devices will provide useful insight into HOW these devices fail. These emerging devices have not been manufactured at scale, so the failure modes have not all been identified, creating a large knowledge gap in failure analysis. With knowledge of the most common failure modes, the manufacturability of these devices can be further improved. Similarly, accelerated lifecycle testing can be done to evaluate the stability of these devices. If significant yield loss is observed during traditional lifecycle testing, then device stability would be identified as a primary concern.

System level Considerations: Ultra-energy-efficient devices will only be widely deployed if they can be integrated into larger systems while retaining their energy efficiency. System level integration, such as advanced packaging and assembly, high-speed interconnects, and system architecture, should be designed to

[8] According to the SRC Decadal Plan, page 43, at its current pace, the demand for memory, roughly 10^{26} bits by 2040, will exceed the projected global silicon supply by roughly 3 orders of magnitude.

maximize the benefit of ultra-energy-efficient devices. Only those ultra-energy-efficient devices that prove to translate to system-level ultra-energy efficiency will be commercialized.

<table>
<tr><th colspan="2">Table 1: Participant Input on Ultra-energy-efficient Devices</th></tr>
<tr><th>Emerging Ultra Efficient Devices</th><th>Performance Metric Tradeoffs</th></tr>
<tr><td>• TFET/Vertical TFET
• CNTFET
• 2D materials—graphene nanoribbons, transition metal dichalcogenides
• FeFET
• PCM
• Spintronic (e.g., SOT-MRAM MESO) devices
• GaN for RF Applications.</td><td>• Speed (frequency, delay)
• Device stability (thermal, mechanical)
• Endurance
• Memory window
• Drive current
• Signal to noise ratio
• Leakage current.</td></tr>
<tr><th colspan="2">Challenges</th></tr>
<tr><td colspan="2">• Establishing robust thermal management of device fabrication to ensure process compatibility.
• Understanding long-term stability and predictability of new materials from first principles.
• Achieving atomically precise deposition and control of new materials.
• Establishing a future path to scaling these devices to manufacturing relevant scales.
• Developing modeling tools to assess tradeoffs of devices, circuits, heterogeneous technologies, and impact on system efficiency and overall performance value.</td></tr>
<tr><th colspan="2">R&D Pathways</th></tr>
<tr><td colspan="2">• Understanding fundamental surface chemistry for the bottom-up fabrication of ultra-energy-efficient devices.
• Engineering materials from earth abundant, easy to extract elements.
• Integrating critical device manufacturing processes for emerging devices with conventional CMOS processes.
• Investigating degradation mechanisms and failure modes of emerging devices.
• Implementing self-limiting chemical processing for abrupt interfaces.</td></tr>
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Ultra-precise Manufacturing Processes

Ultra-precision manufacturing is the next step in a long history of manufacturing at ever-smaller scales. Figure 6 shows the historical progression of UPM (Taniguchi 1983).

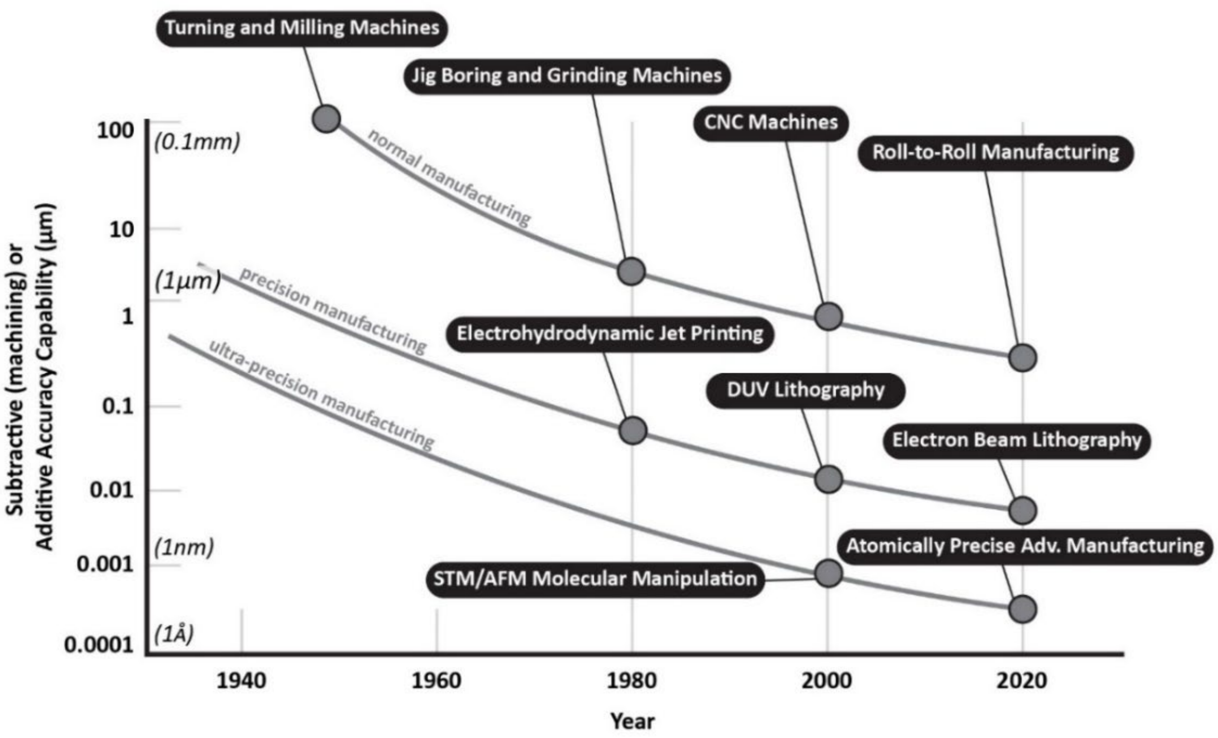


Figure 6: An adaptation of Taniguchi's plot showing the improvements in manufacturing precision over the 20th and 21st centuries. Modified with permission from P. Shore (Shore and Morantz 1973).

While important manufacturing technological advances will continue at larger scales, much that is cutting edge is at the nanoscale, even the atomic scale. As semiconductors devices continue to shrink, atomic precision will be required in material growth, deposition, and etching. The hypothesis that increasing precision and control yields greater energy efficiency is certainly supported by decades of progress in semiconductor manufacturing. Reduction in transistor size, which has led to lower energy consumption, faster operation, and increased transistor count per chip, would not have been possible without increases in manufacturing precision and control. As semiconductor manufacturing technology has become more advanced, UPM has similarly developed, as seen in the figure above.

As noted in the Devices section, the need for ultra-high precision in semiconductors also presents an opportunity for UPM to take advantage of quantum mechanical phenomena such as tunneling, magnetism, and spin. Current UPM processes are undergoing intensive manufacturing R&D to increase accuracy, throughput, and reliability. Near-atomic UPM techniques such as ALD are currently deployed in semiconductor manufacturing environments for high-κ dielectrics and peripheral applications such as environmental coatings. The workshop identified and discussed several UPM techniques, summarized in the section below.

The first UPM processes session consisted of a "plenary interview" between conference chair Tina Kaarsberg (AMO) and Shashank Misra (Sandia National Laboratories), who had just organized a workshop specifically on atomic precision devices, fabrication, and characterization.

The host interview session was followed by a panel session featuring leading researchers in the field, and a facilitated discussion for a deeper, more targeted discussion. The panel consisted of Shashank Misra, Eric Joseph (IBM), Robert Clark (Tokyo Electron, Ltd.), and Raman Achutharaman (AMAT). Shashank Misra discussed atomically precise advanced manufacturing (APAM) and its use in fabricating vertical TFETs to improve current density and subthreshold slope as well as recent results showing the robustness of atomic precision manufactured TFETs. Eric Joseph focused on ALE and how it still is far from an ideal, fully optimized process. Robert Clark emphasized the need to transition to a 3D chip architecture to take advantage of the unused space in the vertical direction. Finally, Raman Achutharaman discussed the tradeoffs in power, performance, area, cost, and time (PPACt) when developing new processes and tools to address the explosion in the number of applications in which semiconductor devices are used.

The following sections integrate the concepts and takeaways discussed during the panel session and facilitated discussion. A more detailed summary of each panel speaker can be found in Appendix B.

Table 2, at the end of the Process chapter summarizes participant input from the facilitated session identifying emerging UPM processes that are likely to make the greatest impact on chip-level energy efficiency in the next years, as well as challenges and R&D pathways for these processes. Table C-4 to Table C-6 includes the full participant input.

Emerging Ultra-Precise Manufacturing Processes

Top-down processes have been the norm in traditional semiconductor foundries. Blanket deposition, optical lithography, and material removal have been the primary processes in IC fabrication since its inception. However, as device dimensions continue to shrink to atomic scales, these techniques are reaching their physical limitations and can no longer provide the precision needed for these devices. This need is fundamentally driving the emergence and widespread acceptance of bottom-up approaches as necessary process steps for the fabrication of next-generation devices.

Many of the most scalable UPM processes that are energy efficient are bottom-up (e.g., self-assembly) approaches that rely on surface chemistry to etch, deposit, or pattern. By harnessing nature's natural preference to minimize energy and associate similar chemical constituents, no matter how small, bottom-up processing techniques make up the bulk of UPM processes.

Area Selective Deposition (ASD): ASD was identified by multiple workshop participants as the UPM process to have the greatest impact on chip-level energy efficiency in the next 10 years. ASD selectively deposits a film in a desired area while inhibiting deposition in others. This inhibition can be done by chemical means, through alterations in surface chemistry via passivation, or physical means, through steric blocking and steering or other surface topography. ASD is typically performed through vapor-phase precursors building layers through vapor-solid reaction processes. CVD and ALD are common methods for ASD. These processes are in principle capable of depositing films with atomic precision, but workshop participants agreed that ASD still does not consistently produce uniform, complete layers and both metrology and improved processes are needed to ensure full coverage required by atomically precise devices.

Atomically Precise Advanced Manufacturing (APAM): APAM is a term coined by researchers at Sandia National Laboratories for their version of hydrogen de-passivation lithography (HDL). HDL is accomplished with scanning tunneling microscopy (STM) instrumentation and removes hydrogen atoms that passivate semiconductor surfaces to create chemically reactive patterns (i.e., dangling bond) with atomic resolution. In the presence of a dopant gas, the dangling bond will preferentially bond with the dopant molecule, allowing for atomic precision in dopant placement. Researchers at Sandia discovered that multiple dopants could be placed at a single site ("ultra-doping") with atomically abrupt doping profiles that drastically improve device performance.

The imaging and lithography modes are performed with the same probe, which allows for a unique capability of closed loop lithography, taking advantage of the surface atomic lattice as a global fiducial grid reducing the metrology task to counting atoms. Recently, ALD scientists have developed an open source "atomiclimits.com database to accelerate work on chemical/process discovery[17]. This database relies on crowdsourcing to make and to keep it up to date and any researcher can add information after a quick evaluation by the content hosts.

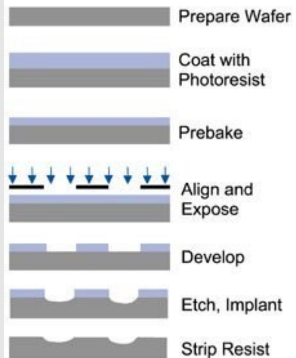
Atomic Layer Etching (ALE): ALE, like ALD, is a self-assembly-driven UPM technique, where precursor molecules are delivered to the reaction chamber and etch a desired surface. However, unlike ALD, ALE is not yet a mature processing technique and further development is needed. In particular, finding the appropriate ALE process window by optimizing ion energy and etch chemistry can improve process throughput and accelerate its adoption in the semiconductor industry.

Top-down vs Bottom-up Processing

Top-down

Top-down processing is a *subtractive* approach where smaller features are formed from larger structures. This has been the standard methodology for the semiconductor industry for the past ~50 years. Typical processes include blanket deposition of metal or dielectric, blanket growth of silicon oxide, and subsequent photolithography and etch of these films. So called edge placement errors are a major bottleneck for fabrication at the smallest scale. Top-down processing is fundamentally limited by the resolution of lithography systems. Currently, extreme ultraviolet (EUV) lithography systems are used in single nm technology nodes but improvements towards atomic-scale precision are increasingly difficult and extremely expensive.

Directed assembling is an emerging top-down approach, where individual atoms can be moved with a scanning probe (i.e., STM, AFM), achieving atomic precision. However, throughput is a major concern.

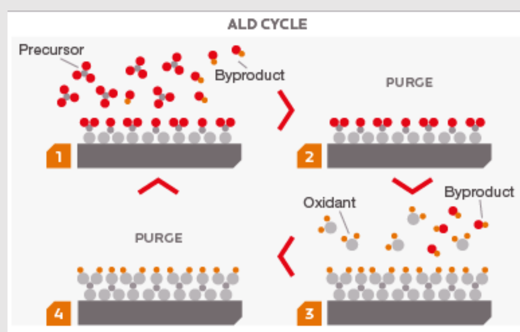


Schematic of a silicon etch and implant process (SPIE).

Bottom-up

Bottom-up processing is an *additive* approach where features are formed through assembling individual constituents (e.g., atoms, molecules, etc.). These processes leverage nature's propensity to aggregate species with similar chemical or biological properties. Because bottom-up approaches allow for assembly through natural, physical forces, structures using this technique tend to have fewer defects and more uniform chemical composition. Typical processes include ALD, ALE, and block copolymers.

Bottom-up processing is limited by the complex and time-consuming nature of designing self-assembling species. The use of atoms or small molecules as the building block provides near-atomic precision in features formed through bottom-up approaches.



Schematic of an ALD cycle showing the self-assembly of species (ASM).

Discussed below are other promising UPM techniques that were not discussed during the workshop but are deployed in industry or used in a research setting.

Lithography

Focused Ion/Electron Beam: Ion or electron beams at high energies can be used to physically cut surfaces with atomic-scale precision; different ions will have different resolutions. These beams can be used for machining tiny features and structures into desired substrates with precision at the level of a few nanometers.

Nanoimprint lithography: Nanoimprint lithography, being essentially a molding process, has much higher precision than competing semiconductor lithography, including EUV (see below), although nanoimprint lithography does not quite have atomic resolution. This technique is already being used for semiconductor memory devices. More accurate templates could be used to produce high-efficiency electronics, possibly including quantum computing devices. HDL has been used to create nanoimprint templates with single-nanometer resolution with much greater accuracy than is possible with any other template-writing technique.

Extreme Ultraviolet (EUV) Lithography: EUV lithography uses a wavelength of light of roughly 13.5 nm. These tools are capable of creating dimensions several nanometers in size but are largely hindered by stochastic phenomena and feature roughness due to shot noise. Samsung and TSMC have already begun integrating these tools into their production lines. However, as device nodes become smaller, the usefulness of photon-based lithography systems must be considered because of the exorbitant cost of new tools, resolution limited by light diffraction, and available photoresist materials capable of such small dimensions (Mojarad, Gobrecht, and Ekinci 2015).

Ultra-Precise Assembly Techniques

Single-Atom Manipulation with STM: The pioneer of STM atom manipulation, Don Eigler from IBM, used an STM tip to position Xe atoms on a Ni surface at 4K, producing, apart from his company logo, quantum corrals that exhibited electron density standing waves (Eigler and Schweizer 1990; Crommie, Lutz, and Eigler 1993). Other notable examples include the work of Sander Otte, who positioned Cl vacancies on Cl/Cu (100) into ASCII codes to spell out the opening sentences of Feynman's "Plenty of room at the bottom" speech (Kalf et al. 2016). This directed assembly technique is capable of atomic-level precision, but the throughput is even worse than HDL.

Atomic Layer Deposition (ALD): ALD is a self-assembly-driven UPM technique. Precursor gases are sequentially pulsed into the reaction chamber to form a film, one layer thick. The precursor gas does not adsorb to itself, creating a self-limiting reaction that has the potential for defect-free, near-atomic resolution. Furthermore, as a chemical deposition technique, ALD (and ALE) can be made selective to a lithography pattern, thus transferring ultra-precise patterns with very high fidelity (Ballard et al. 2014). ALD is starting to be deployed in high-throughput fabs for high-κ dielectrics and its practitioners are increasingly sharing information.[9]

Diblock Copolymer: Block copolymers are composed of discrete blocks of chemically distinct monomer units. When mixed with immiscible block copolymers, they tend to self-assemble with nanometer scale precision. Its versatility, tunability, dimensionality, and feature size make it attractive as a UPM technique (Feng et al. 2017). Recently, researchers created the Block Copolymer

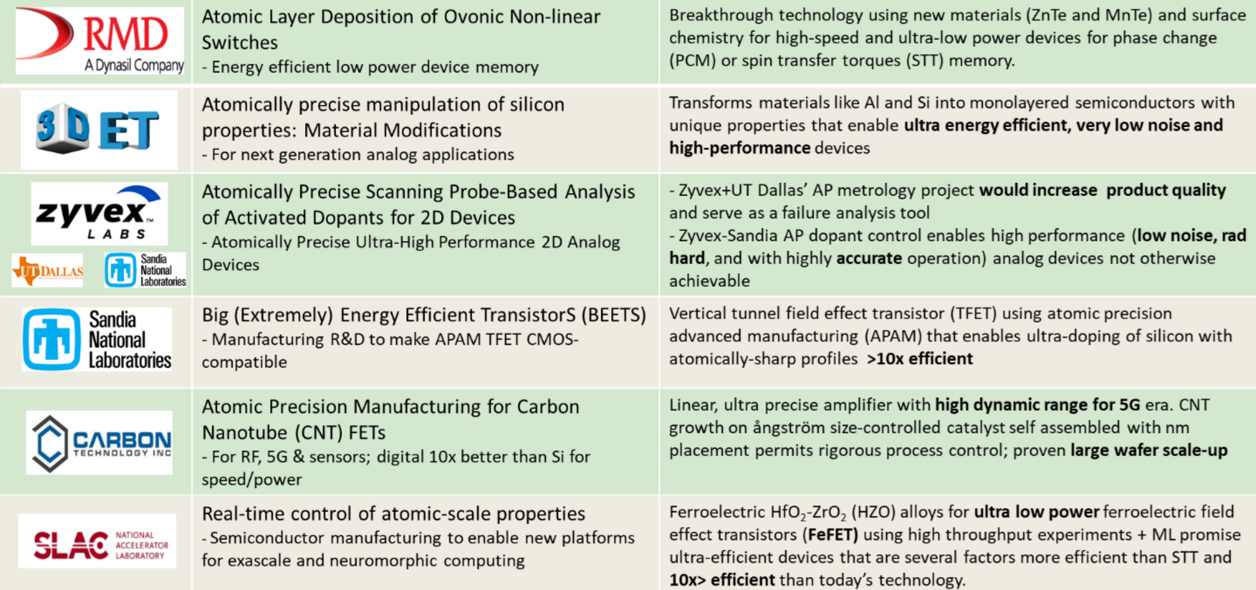
Figure 7. Examples of block copolymers (Feng 2017).

[9] See for example, https://www.atomiclimits.com/2019/03/20/and-here-it-is-the-online-ald-database-a-website-where-you-can-easily-search-browse-and-add-ald-processes/.

Database (BCDB), a collaborative platform that allows users to search, submit, visualize, and download experimental phase measurements and their associated characterization information for di- and multi-block copolymers (BCDB 2020).

Hybrid Bottom-Up Processing: Hybrid bottom-up approaches can leverage multiple facets of UPM techniques to create a versatile manufacturing process. For example, using self-assembly and epitaxy ALD together to alter the surface termination of various regions on the wafer can result in patterned self-assembly without the use of masks or other conventional pattern transfer techniques. These hybrid methodologies may reduce the number of steps required while improving precision. It may be best to do these hybrid techniques within the same tool so as not to expose the wafer to potential contaminants, such as air, halfway through the process. However, this would require custom equipment that has yet to be developed.

AMO's Atomically Precise Manufacturing (APM) program has contributed to the ultra-precision advances that can be applied to semiconductor R&D. Figure 8 summarizes active projects.



Organization	Project	Description
RMD A Dynasil Company	Atomic Layer Deposition of Ovonic Non-linear Switches - Energy efficient low power device memory	Breakthrough technology using new materials (ZnTe and MnTe) and surface chemistry for high-speed and ultra-low power devices for phase change (PCM) or spin transfer torques (STT) memory.
3D ET	Atomically precise manipulation of silicon properties: Material Modifications - For next generation analog applications	Transforms materials like Al and Si into monolayered semiconductors with unique properties that enable **ultra energy efficient, very low noise and high-performance** devices
zyvex LABS; UT Dallas; Sandia National Laboratories	Atomically Precise Scanning Probe-Based Analysis of Activated Dopants for 2D Devices - Atomically Precise Ultra-High Performance 2D Analog Devices	- Zyvex+UT Dallas' AP metrology project **would increase product quality** and serve as a failure analysis tool - Zyvex-Sandia AP dopant control enables high performance (**low noise, rad hard**, and with highly **accurate** operation) analog devices not otherwise achievable
Sandia National Laboratories	Big (Extremely) Energy Efficient TransistorS (BEETS) - Manufacturing R&D to make APAM TFET CMOS-compatible	Vertical tunnel field effect transistor (TFET) using atomic precision advanced manufacturing (APAM) that enables ultra-doping of silicon with atomically-sharp profiles **>10x efficient**
CARBON TECHNOLOGY INC	Atomic Precision Manufacturing for Carbon Nanotube (CNT) FETs - For RF, 5G & sensors; digital 10x better than Si for speed/power	Linear, ultra precise amplifier with **high dynamic range for 5G** era. CNT growth on ångström size-controlled catalyst self assembled with nm placement permits rigorous process control; proven **large wafer scale-up**
SLAC NATIONAL ACCELERATOR LABORATORY	Real-time control of atomic-scale properties - Semiconductor manufacturing to enable new platforms for exascale and neuromorphic computing	Ferroelectric HfO_2-ZrO_2 (HZO) alloys for **ultra low power** ferroelectric field effect transistors (**FeFET**) using high throughput experiments + ML promise ultra-efficient devices that are several factors more efficient than STT and **10x> efficient** than today's technology.

Figure 8: Summary of AMO's APM for microelectronics program

Challenges and R&D Opportunities for Ultra-precise Manufacturing Processes

The increasing complexity of emerging ultra-efficient devices will require more development in ultra-precision processes to manufacture them. Factors contributing to this increase in complexity include:

1. The increasing heterogeneity of materials combinations.
2. The push towards three dimensional devices.
3. The need for ultra-precision in pattern transfer and material interfaces.

At the same time, several process-related challenges hinder the widespread deployment of UPM processes to enable these devices. Summarized below are the challenges and R&D opportunity areas that were discussed throughout the session.

Throughput and scale: At the current developmental stage, many UPM processes forgo throughput to improve precision. However, for widespread industry adoption, UPM processes must achieve similar throughput compared with current VLSI processes. For example, slow throughput is a major concern for STM-based UPM processes, such as APAM, due to the limiting factors of speed and the number of STM tips that the

process relies on. Efforts to improve throughput by developing massively parallel micro-electromechanical system (MEMS)-based STMs for HDL were presented at the workshop (Alipour et al. 2021).

Other promising ultra-precise processes such as ASD do not have the same type of throughput limitations, but are batch processes that have not been demonstrated at manufacturing relevant scales. The chemical reaction physics and fluid dynamics that were optimized at smaller chamber sizes may no longer provide satisfactory performance (e.g., yield drops) when scaling these processes to manufacturing-relevant throughput and scale.

Surface and Precursor chemistry: Many bottom-up UPM processes rely on surface chemistry and chemical reactions of precursor molecules to achieve a desired outcome. A deeper understanding of surface science will better inform researchers on the surface preparation necessary for processing, precursor design to maximize reaction kinetics and material coverage, and other considerations. With such a diversity of chemical precursors, down-selecting the appropriate compound for a specific step in the fabrication process is difficult even with the aforementioned crowdsourced databases and tools. In general, the development of these complex precursor molecules will greatly drive the precision and efficiency of these bottom-up approaches. However, surface chemistry may be just as important in successful processing.

Process compatibility: Lack of compatibility of UPM processes with existing semiconductor fabrication lines was cited as the largest challenge in integrating these processes at foundries. Many of the structures that UPM processes create have limited thermal budget and cannot withstand traditional front-end-of-line (FEOL) processing temperatures. In addition, novel materials and layering schemes used in emerging devices may have chemical and/or structural compatibility concerns when integrating with existing fabrication lines.

Co-design: Utilizing a co-design framework may greatly accelerate the development of the UPM processes and ultra-efficient devices. An interdisciplinary team of researchers (physicists, material scientists, chemists, process experts, design engineers, etc.) may develop more robust and holistic solutions that incorporate traditionally down-stream considerations early in the development process. This can also reduce waste, optimize device design for the foundries' fabrication capabilities, and ultimately improve yield.

AI/ML and modeling: A data-driven approach, leveraging AI/ML, to optimize UPM processes can dramatically reduce the parameter space that researchers will need to physically evaluate by identifying the most prominent process parameters. However, the underlying physical or simulation data upon which these models rely on must be precise and accurate. In addition, the use of high-performance computing can greatly improve modeling fidelity while decreasing modeling time and cost. These *in silico* methods are a powerful tool because they can provide a deeper understanding of the underlying physical mechanisms driving various processes.

Patterning: Some participants asserted that bottom-up patterning techniques that do not rely on light may be the future of atomic scale lithography because they could be much cheaper, produce less waste, and be much more energy efficient than light-based techniques. Throughput and scale up will be the primary challenges to widespread adoption of non-light-based techniques for atomic scale lithography.

Figure 9: Schematic of back-end metal layers. Atomically precise nucleation and termination of via fill is critical to minimize via and interface resistance. Source: Achutharaman, R., 2021

Via fill and interconnects: Vias are gaps etched into the dielectric layers of an IC and filled with metal to connect two conductive layers. Any irregularity introduced in the etching and filling process, such as voids and dishing, can cause resistance to build through each conductive layer, increasing the energy consumption of the device. The dynamic power loss associated with interconnect/via resistance has dramatically increased due to the miniaturization and

growing complexity of semiconductor devices. Via and via interface resistance can be minimized through atomically precise nucleation and termination.

Cost: The extraordinary cost of establishing and operating a foundry makes device manufacturers hesitant to integrate new technologies, especially materials or processes that may be disruptive to their current mode of operation. Transitioning from one material to another in a fab may take years. This outlook against trying new materials or processes often prevents academia or small businesses from being able to use semiconductor foundries for development runs.

Table 2: Summary of Facilitated Session on UPM Processes
UPM processes likely to make the greatest impact on chip-level energy efficiency in the next 10 years
• Area selective deposition • Atomically precise alignment of edges, interfaces, and layers • Selective, monolayer per cycle ALD/ALE • Hybrid bottom-up approaches.
Challenges
• Improving throughput of UPM processes. • Reducing the need for extreme environments in processing. • Ensuring co-evolution of supporting technologies. • Reducing process variability. The smaller things get, the more uniformity is a problem. • Improving chemical and physical stability of atomic level assemblies.
R&D Pathways
• Coupled experimental and modelling approaches to determine selective precursors for ASD. • Multi-disciplinary teams that co-design the next generation of microelectronics. From basic semiconductor science (materials) working with chip developers and experts in computation hardware. • Comprehensive multi-physics modelling in real time. • A systematic study of comparisons between the different processing steps. • AI and machine learning enhanced discovery and design.

UPM Tools and Metrology

Atomic-scale patterning and assembly techniques will require measurement and characterization techniques with sufficient resolution to understand and exploit atomic-scale phenomena. Ultra-precise metrology will be critical in deploying ultra-energy-efficient devices and validating UPM techniques by gaining a more precise view of the underlying atomic structure upon which the devices and UPM techniques depend. However, even techniques with "atomic" resolution, such as transmission electron microscopy (TEM) and atomic force microscopy (AFM), do not provide sufficient resolution to properly characterize atomic structures and require additional advanced metrology techniques. A key takeaway from this panel was that as devices shrink, the number and importance of metrology steps increases, as does the importance of *decreasing process variability*.

There are four times more metrology and inspection steps in a 14nm process than a 65nm process; in addition, processes at smaller scales require more measurement tools. As devices grow smaller in scale, faster time to solution, improving measurement uncertainties, improving measurement precision and resolution, and only measuring what matters will become increasingly important to reduce cost and time spent on metrology.

In-situ metrology helps researchers and manufacturers better understand sources of variability and better control their processes. Furthermore, most metrology and characterization methods used today rely on a modeling step for parameter estimation, and understanding the underlying physics is critical to truly comprehend and make use of the measurements. In addition, hybrid metrology is able to further reduce uncertainties compared with model-based measurements alone by augmenting measurements from model-based techniques to measurements from additional tools. AI/ML can be leveraged with the influx of data from metrology steps to drastically reduce the data stored and transmitted and improve the energy efficiency and security of these metrology steps.

The UPM Tools and Metrology session included a panel session and a facilitated discussion. The panel consisted of Reza Moheimani (University of Texas – Dallas), Bryan Barnes (NIST), Mary Breton (IBM), and Alok Vaid (GlobalFoundries).

Reza Moheimani discussed recent advances in STM that drastically improve its resolution (>10x) of single atoms as a metrology tool and its ability to be used as a lithography tool (100x speedup) to make atomically precise patterns. Bryan Barnes briefly reviewed optical metrology and discussed research opportunities including the use of machine learning, atomistic modeling, and hybrid metrology. Mary Breton gave a general overview of metrology at semiconductor foundries and the metrology trends she's observed, including improving speed/throughput using predictive and hybrid metrology, shrinking spot size through high-power sources, increasing available signals, advanced analytics leveraging machine learning, and transitioning from offline to inline metrology—especially high-end techniques. Finally, Alok Vaid discussed the explosion of metrology and inspection steps in advanced node process lines and highlighted several paths forward, such as reducing measurement uncertainty, acquiring more signal to improve measurement sensitivity, and leveraging hybrid metrology and machine learning, that are necessary to reduce cost and time for large foundries. A more detailed summary of each panel speaker can be found in Appendix B.

Table 3, at the end of this chapter, summarizes participant input from the facilitated session identifying the UPM tools and metrology necessary for UPM processes and R&D challenges and opportunity areas. Table C-7 to Table C-9 includes the full participant input.

Ultra-Precise Manufacturing Tools and Metrology for Ultra-Precise Manufacturing

Below is a summary of common techniques used in semiconductor manufacturing and R&D, most of which were prominently discussed at the workshop.

Optical Metrology: Techniques that rely on light as the measurement medium are often inexpensive, fast, and nondestructive. Light is reflected and scattered, and a sensor collects this light and measures its intensity. Based on the change in light intensity, material constants and other parameters of interest, such as atomic spacing and overlay, can be estimated. Below are three optical metrology techniques often used in semiconductor foundries that will also be useful in UPM.

- **X-Ray Diffraction and variants (XRD/XRF/XRR)**: X-ray diffraction (XRD), X-ray fluorescence (XRF), and X-ray reflectometry (XRR) are all related X-ray based characterization techniques. XRD is used to measure the crystallographic structure of materials and in semiconductor manufacturing is used to study the composition and thickness (nanometer scale) of compound semiconductors and thin films. X-ray fluorescence provides the elemental composition of the sample but does not provide any structural or crystallographic information. X-ray reflectometry is exclusively used to measure thin films on substrates and measures film thickness and surface roughness.

- **Small Angle X-ray Scattering (SAXS):** Measurements of small deviations in radiation from its incident direction caused by interactions with inhomogeneities in matter is the basis of SAXS. SAXS has resolution

down to single-nanometer scale and can determine the shape of nanostructures (Pauw 2013; Orji et al. 2018). Like XRD, SAXS data are in reciprocal space, making structures easier to resolve at smaller length scales, and is especially useful for characterization of advanced node (sub-10 nm) devices. Critical dimension SAXS (CD-SAXS) has been increasingly used as a non-destructive characterization technique for nanostructures, directed self-assembly, and multiple patterning structures. SAXS currently has a very long characterization time and reducing this time is an active area of research (Orji et al. 2018).

- **Scatterometry**: Scatterometry is a non-imaging, model-based optical metrology technique capable of capturing deep-subwavelength size variations through polarization and intensity changes in scattered light. It is a specialized variant of ellipsometry, a technique to measure dielectric properties. Scatterometry is particularly useful in measuring overlay effects, geometric critical dimensions, and optical constants of arrayed structures. Because model fitting to determine desired parameters is reliant on measurement sensitivity and parameter correlation, measurement uncertainties are affected by ambiguities. Parametric correlations, the numerous approximations required, and difficulty determining acceptable uncertainty are the primary challenges of this technique. Despite these challenges, use of scatterometry-based overlay measurements in industry is increasing due to the technique's precision and process compatibility (Orji et al. 2018).

Scanning Electron Microscopy (SEM): Scanning electron microscopes image the surface of a sample by using a focused electron beam and collecting secondary and backscattered electrons. This technique has been shown to provide sub-nanometer resolution. An advanced type of SEM, Critical Dimension SEM (CD-SEM) enables repeatable, non-destructive, and high-speed imaging and metrology through advancements in low electron landing energies, high-efficiency electron detectors, and fast and accurate sample stages. New developments in SEM include sparse and optimized beam-scanning schemes to image only regions of interest; deep learning algorithms for denoising SEM images to enable unprecedented speed and imaging performance; and single-column, multi-beam, and multi-detector SEMs for fast data acquisition. Challenges include limiting error sources such as drift, vibration, beam damage, charging, and contamination; optimizing low-energy operation; and minimizing electron energy variation (Orji et al. 2018).

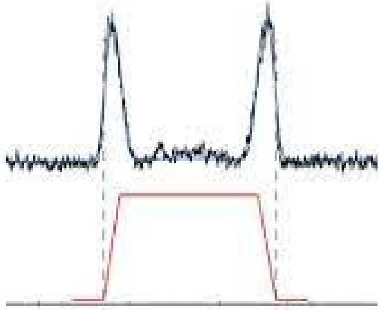


Figure 10. CD-SEM (Villarrubia, Vladar, and Postek 2005)

Transmission Electron Microscopy (TEM): TEM uses electrons transmitted through an ultrathin sample to form an image. Coupling superior spatial resolution with elemental analysis, TEM is particularly useful in characterizing semiconductor device interfaces and structures, crystal structures, film thicknesses, and sub-nanometer features with resolution down to 0.05 nm. Scanning transmission electron microscopy (STEM) has also been used to detect and then reposition impurity atoms in thin Si specimens and graphene. Recent developments include coupling automated focused ion beam (FIB) with STEM to extract site-specific ultra-thin samples for 3D measurements and TEM ptychography, where a number of coherent interference patterns are layered to form an image to evaluate beam-sensitive, low-contrast materials (e.g., CNT, graphene, MoS_2).

Scanning Probe Microscopy (SPM): SPM is a class of microscopy that relies on an atomic probe to scan the surface, measuring changes in physical forces. Four common techniques are summarized below.

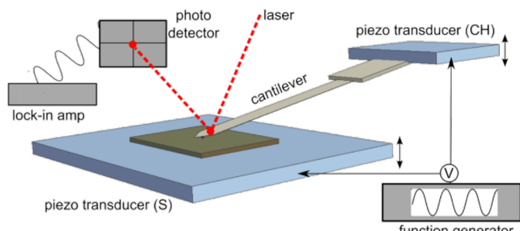


Figure 11. Schematic of an AFM (NIST)

- **Atomic Force Microscopy (AFM)**: AFM is a type of SPM that uses a cantilever with a tip, one atom thick, to observe the surface nondestructively. It can also be used to physically manipulate atoms on the surface, or the surface itself, into desired positions or conformations with single-nanometer precision.

- **Scanning Tunneling Microscopy (STM)**: STM is used to image surfaces with atomic resolution and under different scanning conditions. It can also be used to physically manipulate atoms on the surface, including removing atoms from the surface to create chemically reactive patterns or desired arrangements of atoms on the surface. It is not widely used in industry due to low throughput and the special expertise needed to operate the tool.

- **Kelvin Force Microscopy**: Imaging or relocating buried dopant devices outside of UHV (ultraviolet/visible) systems requires a minimally invasive scanning probe technique. Frequency-modulation Kelvin probe force microscopy (FM-KPFM) allows for the imaging of the surface using a surface potential map, interleaved with a peak-force mode topography scan. The primary advantage of this method is that there is negligible surface oxidation damage because the technique provides the ability to control maximum applied contact force.

- **Tip-based Scanning Near-Field Microwave Microscopy**: This technique is useful in characterizing the electronic properties of metallic and semiconducting materials as well as dielectrics, piezoelectrics, and organic materials down to the nanometer level. Scanning microwave microscopy (SMM), microwave impedance microscopy (MIM), and scanning non-linear dielectric microscopy (SNDM) are all related variants. MIM has been particularly useful in determining CNT type (metallic vs semiconducting) due to its nm resolution (Rubin 2019). Similar to other tip-based approaches, throughput is a major challenge.

Emerging UPM tools and metrology techniques: Summarized below are two emerging metrology techniques that may be particularly useful in UPM. To date, these techniques are mostly used in R&D environments.

- **MEMS-based actuation**: By using a MEMS architecture for the actuators, throughput can be increased with parallel arrays of scanning probes. The technology path and infrastructure to produce massively (millions) parallel arrays of MEMS scanning probes has been explored by Dr. Moheimani and others participating in the workshop (Alipour et al. 2021).

- **Hybrid Metrology**: Statistical hybrid (multi-tool) metrology techniques have been developed to reduce uncertainties for all parameters. Some examples of hybrid metrology include AFM and SEM, AFM and TEM, and CD-SAXS and SEM. Measurement traceability is paramount in a hybrid framework to understand whether measurement divergence from different instruments is due to fundamental differences in measurement physics or to unaccounted-for error sources. Better traceability, standardized parameter definitions, and sample registration methods are needed.

Challenges and R&D Opportunities for Ultra Precise Manufacturing Tools and Metrology

Summarized below are challenges and R&D opportunities that were discussed during the facilitated session.

Translating measurement to device function: Measurements are typically taken on a “metrology” structure that is not part of the active device. As device structures become more complex, the translation and correlation of measurements from these simplistic metrology structures to actual device function becomes increasingly

difficult. Direct measurement is not feasible because it would affect device behavior/performance. Even non-destructive direct techniques, such as SEM, may adversely affect electronically sensitive structures. There is a need to reduce cost and expense of the translation and correlation of measurements from metrology structures to device performance (e.g., threshold voltage, yield, subthreshold slope, etc.).

Reference Metrology: As structures become smaller and more complex, reference metrology is emerging as a gap. The lack of reference metrology reduces traceability of measurements, which in turn reduces the legitimacy of the measurement. TEMs and STEMs are typically used for reference metrology but as devices become smaller and more dependent on the positions or compositions of single atoms, these techniques do not provide enough resolution. More slices can be analyzed but this increases cost and time. Workshop participants noted that significant variability may be introduced through human error during the analysis of TEM images. AI/ML guided analysis may reduce this source of variability, but as of now, most analysis for reference metrology is done by humans.

In-situ Metrology: Controlling wafer-to-wafer process variability in real time without requiring complex control schemes (feedback/feedforward loops) is the main reason for the increased use of in-situ metrology and the leading driver in the explosion of in-situ metrology in advanced node process lines. This capability can greatly reduce variability and improve yield by making adjustments in real time. Progress in this area will require advances in measurement modality, software integration, and tool development for the construction of a physical in-situ metrology module that can seamlessly integrate with a larger tool.

Structure-Geometry Trends: Three trends complicate metrology: (1) smaller size; (2) increased dimensions; and (3) increased integration. As noted earlier, as device size shrinks toward the size of the probe being used, structures become more difficult to image accurately. The complexity of structures increases geometrically as 3D device architectures become more prevalent. Finally, with metrology becoming more integrated into a single tool (so as not to break vacuum), measuring structures or films that are not accessible from the surface or are hidden under pre-existing layers becomes a major challenge. Workshop participants noted, in particular, the difficulty of accessing underlying layers in 3D device architectures with non-destructive techniques. In addition, references for these multi-layered, 3D structures do not exist.

Physics-based modeling: As devices become smaller and many metrology techniques reach their resolution limit, a more detailed understanding of the underlying physics, including electromagnetic, density functional theory, and atomistic modeling, will be critical to correctly estimate parameters needed to make accurate and reliable measurements for emerging ultra-precise metrology techniques. Such models, for example, can generate simulation data for ML.

AI/ML: The explosion in experimental data from the increasing number of metrology steps has presented challenges in processing, storing, and transmitting this data. AI/ML can be used to better estimate parameters using this data as well as simulation data. However, energy consumption and security must also be considered with such large volumes of data being generated. As was discussed in the first Semiconductor R&D for Energy Efficiency workshop on integrated sensor systems, data transmission represents the largest opportunity in the reduction of energy consumption of sensor systems (including sensors systems used in metrology). In well-defined situations common to metrology, the use of AI/ML to only process the necessary data and discard the rest may provide the most efficient means of processing and securing the vast amounts of data from metrology.

Intellectual Property (IP): IP problems were voted most likely to hinder partnerships between device manufacturers and metrologists. Industry and universities now often have strict IP concerns that do not foster collaboration between device manufacturers and the greater metrology research community. Several participants noted the disconnect between pre-competitive research and the practical needs of device manufacturers and suggested that the pre-competitive research formerly fostered by SEMATECH might be an avenue to develop next-generation manufacturing-relevant metrology capabilities. During extended discussion on the importance of IP neutral research agreements that SEMATECH provided in the past, some noted that SRC could support this today while others said that far more resources would be needed than SRC could

provide. It was noted multiple times that getting a fab run to develop new metrology structures that may help the greater semiconductor manufacturing community is very difficult and expensive.

Table 3: Participant input on UPM Tools and Metrology
UPM metrology techniques for ultra-precise manufacturing
• Electron microscopy (SEM, TEM, STEM) • Scatterometry • X-ray-based techniques (XRD, XRF, XRR) • Hybrid metrology.
Challenges
• Understanding and measuring electronic structure and potential changes to electronic structure during processing. • Developing methods to measure structures that are not on or accessible from the surface of the substrate, measuring around corners and underneath pre-existing layers. • Developing more robust interface metrology that can track individual atoms and whether certain processes affect their location. • Measuring thin film and patterned material property constant for a wide array of materials and structures. • Improving in-process sensing.
R&D Pathways
• Leveraging AI/ML to take advantage of the explosion in metrology data. • Developing practical in-situ and integrated metrology solutions for process monitoring that can match or at least approximate the speed of manufacturing. • Establishing metrology centers or institutes. • Optimizing hybrid metrology and the various inputs to get best throughput and measurement uncertainties. • Creating massively parallel systems for combined imaging and deposition.

Non-technical Cross-Cutting Issues

Summarized below are three cross-cutting issues that were brought up in every session and were deemed essential to help drive IP-neutral, precompetitive research that benefits the entire semiconductor community. Table C-10 in Appendix C includes the full set of cross-cutting issues that were identified throughout the workshop.

Access to facilities/equipment: Perhaps the most discussed topic of the workshop, access to state-of-the-art facilities and equipment, was stressed as a severe limitation on the utility of academic and start-up semiconductor research for industry. Academic research labs, where most of the foundational materials, device, and process research is conducted, do not have leading edge fabrication equipment and are typically relegated to using hand-me-down tools that were used in previous nodes (unless custom equipment has been built in house). In particular, many academic cleanroom facilities lack the advanced in-situ characterization equipment that is needed to down-select promising materials for device research. Academic researchers often cannot get access to commercial fab runs to demonstrate their novel technologies due to strict manufacturing schedule and contamination concerns. Progress in semiconductor research would be greatly accelerated if fab access were more widely available. The National Science Foundation held a workshop devoted solely on fab access and as a result has created centers that improve access for academic researchers that were praised by the attendees.

Partnerships with Toolmakers: Nearly all participants cited the importance of government-industry partnerships, and the discussion of partnerships specifically with toolmakers developed several ideas to accelerate the development of next generation devices, manufacturing processes, and tools. Toolmakers are a target because developing the full suite of technologies needed for an advanced node technology is too risky and expensive for fabs. Because toolmakers can develop new capabilities incrementally, aspects of UPM technologies that solve their problems can provide a near-term return on investment (ROI). A research program targeted at government-industry partnerships to help incentivize toolmakers to explore what UPM technologies can do for them—especially in near term bottlenecks related to advanced packaging—was raised as a promising approach by participants. In addition, participants suggested DOE explore innovative funding mechanisms for such partnerships, including prizes and other transactions.

Long-term, Comprehensive Programs: Establishing long-term (5-10 years) research programs that address a breadth of topics, including materials science, surface chemistry, circuit design, and manufacturability, would better leverage research results and might greatly accelerate the development and deployment of ultra-efficient devices, UPM processes, and UPM tools and metrology. The typical two-to-three-year funding cycle does not normally allow for R&D needed for transformational hardware technologies examined during this workshop. A five-year project length with a five-year option was proposed as a potential alternative to the current project structure. Participants noted that since 2018, small business innovation research/small business technology transfer (SBIR/STTR) grants have had the option to extend as long as eight years and that interagency SBIR/STTR might be useful for such projects. Other participants suggested a benchmarking study may need to be completed to assess the energy efficiency of various devices and processes and understand the true economic and energy impacts of proposed technologies before a long-term program in this area is undertaken.

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Appendix A: Agenda

DAY 1: April 21, 12:30 PM – 5:30 PM EDT	
Time	**Activity**
12:30 – 1:00	**Opening Plenary**
12:30 – 12:35	Welcome from DOE AMO Organizers (Tina Kaarsberg, AMO, UPC4UED Workshop Chair)
12:35 – 1:00	Welcome from Biden/Harris Administration & Q&A (Kelly Speakes-Backman, Acting Assistant Secretary, Office of Energy Efficiency and Renewable Energy)
1:00 – 1:30	Semiconductors and Manufacturing are Mutually Essential (Todd Younkin, President & CEO, Semiconductor Research Corporation (SRC))
1:30 – 2:20	**Federal Panel on Semiconductor Device Research (Tina Kaarsberg, AMO, Moderator)**
1:30 – 2:00	- Andrew Schwartz, DOE, Office of Science - Curt Richter, DOC, NIST - Lloyd Whitman, National Science Foundation
2:00 – 2:20	Panel Q&A on Federal Role in Semiconductor Device Research
2:20 – 2:30	**BREAK**
2:30 – 2:50	**How to get 10^6 more semiconductor energy efficiency (Victor Zhirnov, Chief Scientist, SRC)**
2:50– 3:50	**Ultra-Energy-Efficient Devices Panel (Paul Syers, AMO, Moderator)**
2:50 – 3:30	- Alan Seabaugh, UND, logic devices - Dmitri Nikonov, Intel, logic devices especially magnetic spin-orbit - Carlos H. Diaz, TSMC, memory especially FeFET - David Howard, Tower Jazz, RF and communications
3:30 – 3:50	Panel Q&A on Ultra-efficient Devices
3:50 – 4:00	**BREAK**
4:00 – 5:00	Facilitated Discussion on Ultra-efficient Devices (Emmanuel Taylor, Energetics, facilitator; Paul Syers, AMO, and Alan Seabaugh, UND, co-chairs)
5:00 – 5:20	Report outs on Ultra-efficient Devices and General Discussion
5:20 – 5:30	**Concluding Remarks (Tina Kaarsberg, AMO, UPC4UED Workshop Chair)**

DAY 2: April 22, 12:30 PM – 5:30 PM EDT	
Time	**Activity**
12:30 – 12:50	**Welcome, Report out from SNL APAM Workshop, Panel Charges (Tina Kaarsberg, AMO)**
12:50 – 1:50	**Ultra-Precise Manufacturing Processes Panel (Tina Kaarsberg, AMO, Moderator)**
12:50 – 1:30	- Shashank Misra, Sandia National Laboratories, APAM TFET manufacturing - Eric Joseph, IBM, Atomic Layer Deposition, Etching and Selective Area Deposition - Robert Clark, Tokyo Electron, Manufacturing for Energy Efficient Devices - Raman Achutharaman, Applied Materials, Ultra Precision Manufacturing.
1:30 – 1:50	Panel Q&A on Ultra-Precise Manufacturing Processes
1:50 – 2:00	**BREAK**
2:00 – 3:00	Facilitated Discussion on Ultra-precise manufacturing process (Emmanuel Taylor, facilitator; Tina Kaarsberg, AMO, and John Randall, Zyvex Labs, co-chairs)
3:00 – 3:10	**BREAK**
3:10 – 4:10	**Ultra-Precise Manufacturing Tools and Metrology Panel (Rick Silver, NIST, Moderator)**
3:10 – 3:50	- Reza Moheimani, UT-Dallas, Innovations in Imaging, Spectroscopy, and Lithography with STM - Bryan Barnes, NIST, Overview of Metrology for Semiconductor Devices Part 1 - Mary Breton, IBM, Overview of Metrology for Semiconductor Devices Part 2 - Alok Vaid, Global Foundries, Overview of Metrology for Semiconductor Devices Part 3
3:50 – 4:10	Panel Q&A on Ultra-Precise Manufacturing Tools and Metrology
4:10 – 4:20	**BREAK**
4:20 – 5:20	Facilitated Discussion on Ultra-precise manufacturing tools and metrology (Emmanuel Taylor, facilitator; Rick Silver, NIST, and Bryan Barnes, NIST, co-chairs)
5:20 – 5:30	**Day 2 Concluding Remarks (Tina Kaarsberg, AMO, UPC4UED Workshop Chair)**
DAY 3: April 23 12:30 – 5:30 EDT	
12:30 – 12:35	**Welcome Back (Tina Kaarsberg, AMO, UPC4UED Workshop Chair)**
12:35 – 1:35	**Report Outs from UED, UPM and UPTM Facilitated Discussions on Day 1 and Day 2**
12:35 – 12:55	Ali Keshavarzi and Paul Syers, co-chairs, Ultra-Energy-Efficient Devices
12:55 – 1:15	John Randall and Tina Kaarsberg co-chairs, Ultra-Precise Manufacturing Process
1:15 – 1:35	Rick Silver and Bryan Barnes, co-chairs, Ultra-Precise Manufacturing Tools and Metrology
1:35 – 1:45	**BREAK**
1:45 – 3:15	**Priority Research Directions Discussion UPC4UED and Beyond (Tina Kaarsberg, AMO)**
1:45 – 2:45	Discussion on Priority Research Directions for UPC4UED (Tina Kaarsberg, AMO)
2:45 – 3:15	Next Steps—UPC4UED + WHAT for Ultra-efficient Computing (Sadas Shankar, Harvard)
3:15 – 3:30	**Workshop Concluding Remarks and Thank You (Tina Kaarsberg, AMO)**

Appendix B: Plenary and Panel Talk Summaries

Day 1

Welcome from Biden Administration – *Kelly Speakes-Backman, Acting Assistant Secretary, DOE EERE*

Kelly Speakes-Backman discussed the Biden Administration's climate and energy goals and the role that innovation in semiconductor manufacturing can play in achieving these goals. The Administration has set an ambitious goal of transitioning to a 100% clean energy economy by 2050. Ms. Speakes-Backman noted that the key to reaching this goal will be the electrification of industry to achieve net-zero emissions. Semiconductor devices power almost every aspect of modern life and much of the nation's critical infrastructure cannot function without them. In addition, widespread, sustainable electrification of the world's economy and industry will require additional semiconductor deployment across a wide and diverse application space. However, because semiconductors require electricity to function, this explosion in the use of semiconductor devices has led to unsustainable energy consumption and has become a major contributor to the climate crisis.

The semiconductor industry is at an inflection point where federal investment in manufacturing technologies could enable the transition towards the production of dramatically more energy-efficient devices. This transition could help lead the semiconductor industry towards a more sustainable path of energy consumption in semiconductor products and help the industry become part of the solution to climate change. Not only will these investments improve the energy efficiency of semiconductor devices, but it will also help bolster the domestic semiconductor manufacturing industry by increasing the competitiveness of domestic device and chip manufacturers. Acting Assistant Secretary Speakes-Backman praised the Advanced Manufacturing Office's (AMO's) research to date on ultra-precise control for ultra-energy efficient manufacturing and called out AMO's Sandia project on tunneling field-effect transistors (TFETs) as an example of research that should be pursued. She noted that commercialization of ultra-energy-efficient devices, like TFETs, would ripple through the entire semiconductor industry and supply chain and complement efforts to achieve ultra-energy efficiency through new architectures and software to reach the goal of million-fold energy efficiency increase proposed by the Semiconductor Research Corporation (SRC). With this, semiconductors can go back to being a part of the solution for the climate crisis.

The Administration's American Jobs Plan called for $50 billion in semiconductor manufacturing and research at DOE and other agencies. In addition, President Biden issued an Executive Order to secure and strengthen America's supply chains, including identifying risks in the semiconductor manufacturing supply chain. With these actions, the Administration intends to secure the United States' position as the innovative leader in semiconductor research and expand the country's capabilities in semiconductor manufacturing.

Semiconductors and Manufacturing are Mutually Essential – *Todd Younkin, President and CEO, SRC*

Todd Younkin, President and CEO of SRC, gave a wide-ranging talk entitled "Semiconductors and Manufacturing are Mutually Essential." He began by noting that in January 2020, the World Economic Forum reported that climate change had beat out cybercrime and financial crises as the top risk facing the world. He went on to discuss how SRC was addressing the climate threat as well as the global COVID-19 pandemic and growing tensions from socio-economic, racial, and political divides and nationalism. He started with opportunities such as sustainable computing and communications, including data movement and the memory wall as well as Industry 4.0—robotics, automation, and advanced manufacturing. He agreed with the workshop organizers that continued, cost-effective breakthroughs in hardware—including in materials and advances in 3D monolithic and heterogeneous integration; systems that meet the needs of extreme environments, including cryo, auto, and space; architectures that address the compute and memory divide; and accelerated and automated design and validation tools for analog, mixed signal, and digital—were foundational to the future.

He went on to discuss SRC's current partnerships with government (DOD/DARPA, DOC/NIST and NSF); 21 companies (AMD, Analog Devices, ARM, Intel, Samsung, Qualcomm, TEL, etc.); 100+ universities; and 800+ industry liaisons. He noted that in 2020, SRC funded $95M+ in collaborative research at 90 U.S. and 38 international universities in 14 countries. He noted that the Jan 2021 SRC Decadal Plan for Semiconductors fit in with a host of similar earlier documents such as DARPA's 2017 ERI plan and the Semiconductor Industry Association (SIA) 2019 Blueprint.

Dr. Younkin then gave several examples of the what SRC already has contributed to ultra-precise manufacturing (UPM) research, including extensive work on block copolymers (BCPs) to shrink patterns that were commercialized by SRC partners such as IMEC; metrology (e.g., CD-SEM, MMSE* scatterometry, and critical dimension small angle X-ray scattering) to characterize nanowire/nanosheet field-effect transistors (FETs); device and circuit benchmarking through SRC's NRI and STARnet Programs in 2013–2018; and research on p-bits for quantum computing.

Future efforts are based on the Roadmap (SRC 2.0) that envisions a 3x increase in government investment (to $34B through 2030) in semiconductor research and development (R&D) based on addressing the five grand challenges: analog data deluge, memory and storage growth, communication capacity and data generation needs, information and communication technology (ICT) security, and planetary compute energy.

Federal Panel

The U.S. government engages in a wide array of semiconductor R&D, with a multitude of agencies and offices funding mission-specific R&D efforts. To contextualize the workshop within the greater federal semiconductor R&D ecosystem, a federal panel, consisting of representatives from the DOE Office of Science (SC), the National Science Foundation (NSF), and the National Institute for Standards and Technology (NIST), provided an overview of their respective agency or office and discussed the (often overlapping) mission space of semiconductor R&D within their agency or office.

Andy Schwartz, DOE Office of Science: Dr. Andy Schwartz gave an overview of DOE Office of Science (SC) and its microelectronics R&D efforts. SC has been at the leading edge of microelectronics research for decades, both as a consumer and as a driver of scientific understanding that has enabled many technological breakthroughs. These breakthroughs have been implemented at many SC facilities from high performance computing (i.e., supercomputers) to the instruments necessary in particle physics accelerators found at national laboratories. To enable the next-generation microelectronic devices, SC held a workshop and published a report on Basic Research Needs for Microelectronics that stressed the importance of a co-design framework that allows for multi-directional information flow across the stack to overcome traditional barriers to innovation. Dr. Schwartz closed by highlighting the microelectronics research that SC funds, including fundamental studies in materials science, chemistry, and physics; novel device structures and integration schemes; and algorithms, programming, and system architecture modeling. SC funds most of its microelectronics research through five offices: Advanced Scientific Computing Research, Basic Energy Sciences, Fusion Energy Sciences, High Energy Physics, and Nuclear Physics.

Curt Richter, NIST: Dr. Curt Richter gave an overview of NIST and its microelectronics R&D efforts. NIST, within the Department of Commerce, has a unique mission to promote innovation and competitiveness by advancing measurement science, standards, and technology and is the only entity to do so. Their primary mission is to develop and disseminate measurement standards to ensure measurements made by industry are traceable back to the International System of Units (SI) standard. In addition to providing measurement science, NIST has been a leader in delivering foundational scientific knowledge. They have put particular focus on five critical industries of the future: quantum science, artificial intelligence (AI), advanced communications, advanced manufacturing, and engineering biology. All of these critical industries are related and coupled with microelectronics. NIST has a long history of developing the most advanced nanoscale fabrication and characterization methods that provide the foundation to make, measure, and model practical atomic devices for future classical computing and quantum computing, sensing, and analogue simulations. Dr.

Richter closed by highlighting impactful public-private partnerships that NIST engages in; in particular, nCORE, organized and operated by SRC, NIST, and NSF.

Lloyd Whitman, NSF: Dr. Lloyd Whitman gave an overview of NSF and its microelectronics R&D efforts. NSF supports basic research (including solutions-oriented, use-inspired research), research infrastructure, and education and workforce development to advance the full stack associated with semiconductor materials and devices and their integration into systems. This support is provided through programs administered by multiple NSF directorates and Offices, including programs conducted in partnerships with other agencies and industry to further nurture innovative ideas and develop a skilled workforce. Dr. Lloyd closed by highlighting NSF's current semiconductor related programs including materials development for novel, biological devices, development of energy-efficient devices and architectures, and an industry approved semiconductor manufacturing apprenticeship program.

How to get 10^6 more semiconductor energy efficiency – *Victor Zhirnov, Chief Scientist, SRC*

Dr. Victor Zhirnov discussed the current trajectory of computational energy use and offered a potential path forward to reduce this energy use by 1,000,000x. Dr. Zhirnov opened his talk by providing an overview of the recently released Decadal Plan for Semiconductors, a joint publication by SRC and the SIA. The report highlights five areas where seismic shifts are necessary to continue to drive innovation in ICT: analog, memory and storage, communication, security, and computational energy.

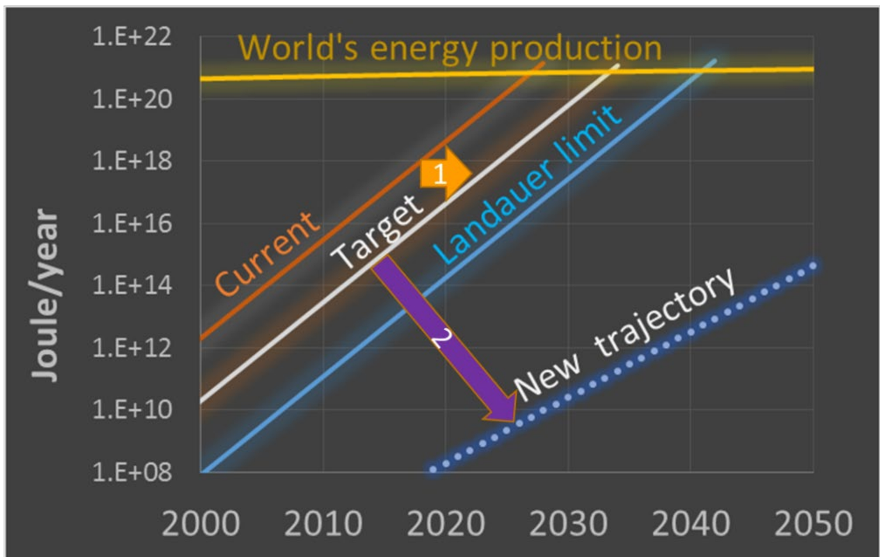

Figure 12: Various trajectories of computational energy use. "Current," "Target," and "Landauer limit" utilize the traditional computational paradigm, with a bit utilization of 2/3, and will hit the world's energy production in the coming decades. Radically new computing paradigms such as quantum and neuromorphic computing and AI engines will push us towards the "New trajectory." Source: Zhirnov, V., 2021

With the explosion of computational devices, the sheer amount of information generated has grown exponentially. While the energy per bit has exponentially decreased over time, the number of computations has grown at a faster rate, pushing us towards an unsustainable path of energy use. Developing technology under the current paradigm will not be enough to shift computational energy use towards a more sustainable path. As seen in Figure 12, even if we achieve the theoretical limit of computational energy use under the existing paradigm, known as the Landauer limit, semiconductor energy use would equal the entire world's energy production by 2040.

In order to avoid the planetary energy production and achieve 10^6 times improvement in energy efficiency in computation processes, a radically different computing paradigm with a much higher bit utilization is necessary, as shown in the "New trajectory" line in Figure 12. He noted that in some applications the human brain is as fast as a supercomputer but uses 1,000,000x less energy. Hence the human brain is a promising alternative model to push the computational trajectory on a more sustainable path having 10^6 more energy efficiency.

Ultra-efficient Devices Panel Discussion

Alan Seabaugh, University of Notre Dame: Dr. Alan Seabaugh discussed two promising, ultra-efficient emerging devices: the tunneling FET (TFET) and the ferroelectric FET (FeFET). A 2015 benchmarking study commissioned by the SRC, Figure 13, showed that tunneling FETs are consistently faster with lower energy than conventional and other emerging devices. By applying a voltage to the gate, the potential of the conduction band is lowered enough that charge carriers in the valence band are able to directly tunnel through the barrier. The primary advantage of the TFET mechanism is that the subthreshold slope isn't constrained by thermal energy and therefore is able to achieve subthreshold slopes less than 60 mV/decade, which is standard for silicon devices. The primary challenges for TFETs are manufacturing challenges associated with sub-nanometer equivalent oxide thicknesses and extremely precise alignment, the creation of proper doping profiles for the tunnel junctions, and the difficulties in integrating with back-end-of-line processes.

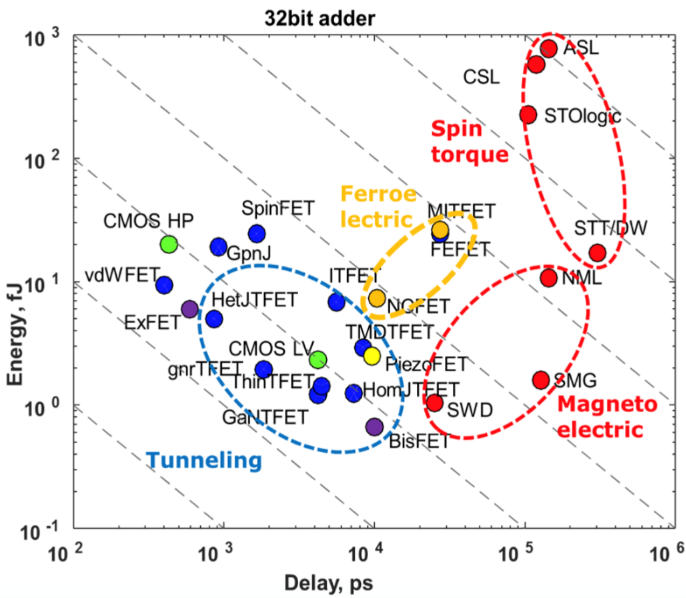

Figure 13: Benchmarking study showing the switching energy vs delay of emerging devices, TFETs, FeFETs, and magneto-electric, compared with state-of-the-art silicon devices, green dots (Nikonov and Young 2015).

FeFETs are a promising, emerging memory device that could also be used for logic. FeFETs rely on a ferroelectric material under the gate electrode that is able to switch polarization as a voltage is applied. The primary challenges for this device are hysteresis of the ferroelectric layer, cycling endurance, the presence of a sub-oxide layer between the ferroelectric and silicon surface, and the polycrystalline grain structure of the ferroelectric.

Dmitri Nikonov, Intel: Dr. Dmitri Nikonov discussed magneto-spin orbit (MESO) devices and their promise as an ultra-energy-efficient logic device. MESO devices operate by the magnetoelectric effect, in which a voltage applied to the device alters its magnetic properties. This change in magnetization is able to generate a current through the spin-orbit effect. These two principles help lower operating voltage and lower energy consumption of the device. Dmitri stressed that although these devices are slower than traditional memory devices, they have a smaller energy footprint, which makes them attractive for use in future systems. He highlighted that there is a precedent for trading off speed for energy efficiency, as seen during the transition from BJTs to complementary metal-oxide semiconductor (CMOS) devices, and that speed is not the only factor when considering new devices.

Carlos H. Diaz, TSMC: Dr. Carlos Diaz opened his remarks by highlighting that technological advancement is necessary to reduce computational energy use while sustaining computing capacity growth. While memory system performance is being addressed by 3D integration, he noted that low complexity memory installed in computers may be the new frontier on the device level. However, any emerging memory device must meet all critical metrics for state-of-the-art devices, including memory window, density, speed, endurance, retention, and error rates. He highlighted five promising memory devices, STT-MRAM, SOT-MRAM, Fe-RAM, PCM, resistive random-access memory (RRAM), and ECRAM. The goal of research on emerging devices is to identify fundamental showstoppers and areas of improvement to further advance these devices. Dr. Diaz closed with a discussion on crossbar memory arrays. This architecture can greatly enhance memory density but has challenges, beyond the constituent memory elements, particularly in terms of scalable selector devices having

high enough on-off current ratio and speed, good thermal stability, low variability, and robustness against long-term parametric drift, among others.

David Howard, TowerJazz: Dr. David Howard gave an overview of TowerJazz and highlighted two application areas, radio frequency silicon-on-insulator (RF-SOI) and radio frequency CMOS (RF-CMOS), where next-generation analog devices are necessary. TowerJazz specializes in analog electronics with a large customer base and focuses on three primary areas: RF-SOI and RF-CMOS, producing devices for switches, antennas, and power conditioning; silicon germanium (SiGe) and bipolar CMOS (BiCMOS) producing devices for data centers, WiFi, and high frequency applications; and silicon photonics, a new business area, which focuses on developing photonic devices. Dr. Howard then discussed the data center and mobile phone markets as key drivers for advanced analog electronics. Each application area has an associated roadmap, (e.g., 4G, etc. for the mobile phone market) and figures of merit that push innovation forward. Dr. Howard noted that in analog electronics, customers care more about performance than energy efficiency and therefore improvements to energy efficiency typically occur as a byproduct of improved performance.

Day 2

Report-Out from Sandia National Laboratories Workshop on Atomic Precision, Tina Kaarsberg and Shashank Misra

Dr. Tina Kaarsberg and Dr. Shashank Misra had a conversation regarding Sandia National Laboratories' Workshop on Atomic Precision. Dr. Misra, the organizer of Sandia's Workshop on Atomic Precision, is the principal investigator of Sandia's FAIR DEAL Grand Challenge and AMO's Big Energy Efficient Transistors (BEETS) project. Although organized separately, the two workshops discussed the same three workshop topics: devices, manufacturing, and tools and characterization, because of their highly overlapping and related nature.

Before discussing the takeaway and conclusions of the Sandia workshop, Dr. Kaarsberg reviewed AMO's current portfolio on ultra-efficient devices and UPM processes and tools and characterization and jointly classified each project into one of the three categories. A conclusion of this exercise was that often projects are relevant to more than one category. Currently, there are seven projects related to these topics, in addition to six more related projects in atomically precise manufacturing.

Dr. Kaarsberg and Dr. Misra then discussed the major takeaways from the Sandia workshop. In particular, Dr. Misra highlighted the interrelationship between fabrication, characterization, and devices. At the atomic scale, there are significant opportunities that emerge from the intersection of all three topics. Dr. Misra stressed the importance of finding a strong application driver for a given technology to achieve critical mass and attract robust funding for foundational research efforts. Finally, it's important to connect basic science research with real world problems. The practical application of basic science research will only attract more funding opportunities to further learn and develop innovative technologies.

Takeaways from the Sandia National Laboratories Workshop on Atomic Precision

Devices

- Beyond performance, factors like robustness are important to understand in deploying technologies. For example, accelerated lifetime testing shows APAM and CMOS have comparable robustness.
- Self-limiting processes are needed to gain control over variations at small scales.
- New electronic properties emerged with confinement in devices based on metal chalcogenide ALD films and nanowires.
- Vertically integrated teams are needed due to the interdependence of advanced technologies in microelectronics.

Near-Atomic Fabrication

- Challenges arise with edge placement, film thickness nonuniformity, and film integrity as features shrink.
- ALD/ALE have inherent randomness and defects, which result in films that are not atomically precise.
- ALE needs to accommodate a wide range of processes needs.
- Hybrid metrology improves spatial resolution compared with single tool characterization techniques.
- Self-limiting bottom-up processing techniques are an interesting direction for atomically precise manufacturing.

In-operando Characterization at the Atomic Limit

- Atomically precise devices are a lot easier to fabricate than to characterize.
- Synchrotron light sources average over an area but offer multimodal characterization. The use of lenses has allowed <10nm spatial resolution.
- Many opportunities exist for combining physics-based modeling and transmissions electron microscopy.
- Many opportunities exist for in-operando characterization.
- AI/ML can be leveraged to improve real-time characterization.

Ultra-Precise Manufacturing Processes Panel Session

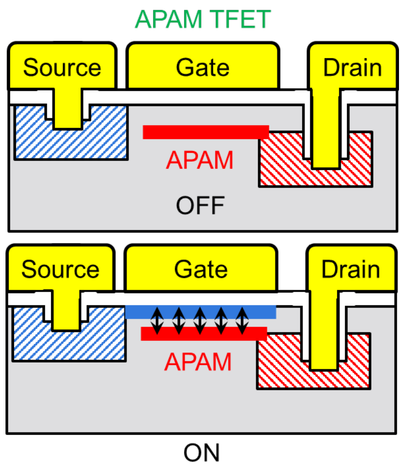

Figure 14: Schematic showing the operating mechanism of the vertical TFET. Source: Lu, IEEE Nanoelectronics Workshop, 2021

Shashank Misra, Sandia National Laboratories: Dr. Shashank Misra discussed atomically precise advanced manufacturing (APAM), an UPM technique developed at Sandia National Laboratories, and its application in the fabrication of TFET devices. APAM uses a scanning tunneling microscope to selectively remove hydrogen atoms from a silicon surface creating an atomically precise pattern of dangling bonds. The introduction of dopant gas, such as phosphine or diborane, allows for atomic control of dopant placement. Sandia is using this technique to fabricate vertical TETs that will achieve steeper subthreshold slope and lower operating voltage compared with conventional silicon devices and might thus be a potential drop-in replacement for CMOS. A 10x increase in energy efficiency has been predicted for these devices. Dr. Misra closed by discussing the manufacturability roadmap for APAM TFETs. For widespread adoption of APAM TFETs, wafer-scale manufacturability will be paramount. In order to accomplish this, a strong application driver must be identified in order to garner enough interest in the technology to enable the development of a specialized, high-throughput APAM tool.

Eric Joseph, IBM: Dr. Eric Joseph discussed atomic layer etching, deposition, and selective area deposition for UPM. He gave particular focus on the developments needed in ALE to further enhance its capabilities as an UPM process. As device nodes have become smaller, innovation has been the main driver in the continuation of Moore's Law. Each smaller device node introduces greater challenges to processing that require new materials or device structures. Today, many devices require atomic scale processing. ALD and ALE are used in many of the largest fabs. However, a number of innovations are still needed—in particular, ALE. Finding the process window for ALE will enable true atomic scale precision of ALE processes. Ion energy and chemistry optimization are two parameters that can be investigated to achieve the required process window. There is significant research in both of these areas. Once the process window has been established, true atomic layer precision will be achieved. Dr. Joseph closed by highlighting examples where true atomically precise ALE can benefit semiconductor processing, including 2D/carbon material processing, self-aligned processing with carbon nanotubes and graphene, area selective deposition, and emerging memory implementations.

Robert Clark, Tokyo Electron, Ltd.: Dr. Robert Clark discussed the need to transition to a 3D chip architecture to take advantage of the unused space in the vertical direction. Semiconductor manufacturing has relied on 2D architectures since its inception and steady improvements in materials and device designs have enabled the continuation of Moore's Law and Dennard Scaling. However, this continuation has lost steam in the last 15 years. With this, memory has begun to utilize the third dimension and logic needs to go in this direction as well. In a 2D architecture, transistors take up roughly 70% of the chip area. As the fundamental limit of scaling of individual devices has been reached, more transistors cannot be put down in the chip area. However, in a 3D orientation, only 1.4% of the space is utilized by chips. Stacking devices

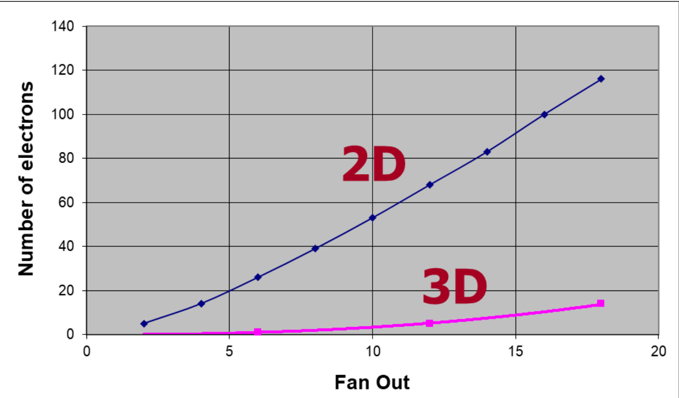

Figure 15: 3D devices can achieve larger fan out (branching) while using a smaller number of electrons (i.e., energy consumption) due to its 3D architecture. A 10x energy reduction is observed in fanout of 4–6. Source: Clark, R., 2021 (adapted from Zhirnov, Victor and Ralph Cavin. 2015. "Microsystems for Bioelectronics: Scaling and Performance Limits." Elsevier).

can more than the double the number of devices in the same 2D area. A 3D switch is much more energy efficient than a 2D switch due to its ability to achieve larger fan out, as seen in Figure 15. How 3D architecture will be implemented in a logic framework is still unknown. In order to achieve robust device performance utilizing a 3D architecture, atomic precision will be required in patterning, layer alignment, and interfaces. Dr. Clark closed by highlighting opportunities in 3D systems, including proximity of memory and logic devices, reduction of interconnects due to its ability to stack devices on top of each other, and increase in fan out equating to more computations per step.

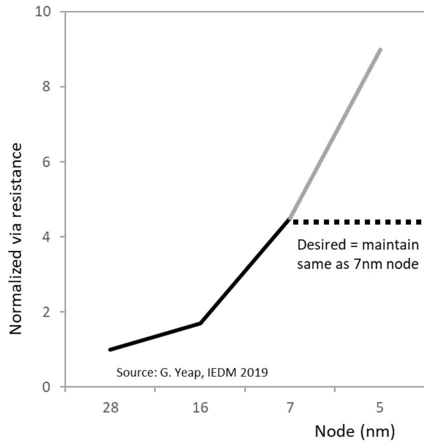

Figure 16: Via resistance increasing dramatically as node shrinks. Source: Achutharaman, R., 2021

Raman Achutharaman, AMAT: Dr. Raman Achutharaman gave an overview of AMAT and discussed the tradeoffs in power, performance, area, cost, and time (PPACt) when developing new processes and tools to address the explosion in the number of applications in which semiconductor devices are used. AMAT has been developing semiconductor tools and capabilities for over 50 years and spends roughly $2.2 billion in R&D of next-generation technologies. Their technologies have made an impact from atomic-scale devices to industrial-scale wafer/device manufacturing. There have been four eras of growth in the semiconductor industry: mainframe, starting in the early 90's; PC and internet, starting in the early 2000's; mobile and social, starting in the late 2000's; and AI/big data starting in the late 2010's. This latest era has seen an explosion in the number of devices and diversification of applications that semiconductor products are used in. With this, PPACt must be optimized to meet customer needs while keeping costs realistic. New architectures, structures, materials, strategies to shrink devices, and advanced packaging can be leveraged to achieve this goal. Interfacial resistance was highlighted as a major scaling roadblock that must be overcome to enable future devices, Figure 16. Dr. Achutharaman closed by highlighting AMAT's recent integrated platform tool with nine process chambers and a metrology chamber to complete an entire via fill and reflow process without breaking vacuum.

Ultra Precise Manufacturing Tools and Metrology Panel Session

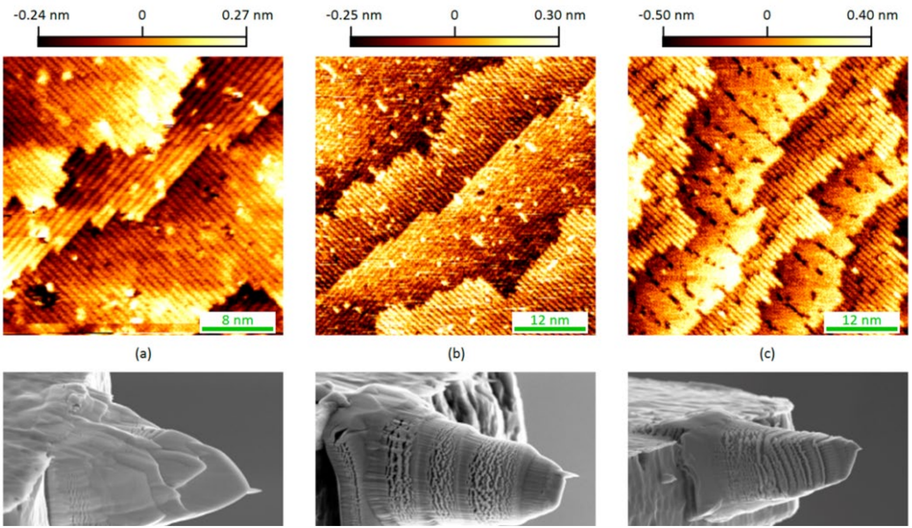

Figure 17: Images of hydrogen terminated Si(100) acquired from three different MEMS devices. Image quality is comparable to conventional STM. Source: Moheimani, R., 2021

Reza Moheimani, UT – Dallas: Professor Reza Moheimani discussed his recent advances in scanning tunneling microscopy (STM) and how his souped-up STM can be used as a metrology tool for single atoms. He also noted its usefulness as a lithography tool to make atomically precise patterns. Although STM was first introduced decades ago, much of the hardware and software hasn't changed in the past 40 years. Yet it is still considered to be the best

tool to study conducting and semiconducting materials at the atomic limit. Dr. Moheimani and his team have changed the hardware and software configuration of the STM to improve resolution and accuracy 10x. He provided a comparison image where conventional STM showed a grainy image in the first derivative of a current vs. voltage (IV) measurement, and completely unresolved images for the second and third derivative. The improved STM shows very clear images for the first, second, and third derivative. By varying the feedback control method, IV data can be acquired on the fly, compared with hours for a standard STM tool. Using the improved STM, Dr. Moheimani and his team have demonstrated hydrogen de-passivation lithography, a method of atomically precise lithography that plucks single hydrogen atoms off a silicon surface. Finally, a MEMS-based STM scanner is being developed that can improve tool throughput another order of magnitude by parallelizing the scanning process, while maintaining a comparable image resolution, Figure 17.

Bryan Barnes, NIST: Dr. Bryan Barnes briefly reviewed optical metrology and discussed the challenges and research opportunities to advance the metrology field, including the use of machine learning, atomistic modeling, and hybrid metrology. In optical metrology, a beam of light is emitted at a sample, where it is reflected and scattered. It is the workhorse of most fabs due to its inexpensive, fast, and non-destructive operation. He also mentioned the use of electrons rather than photons as probes. The changes in intensity and wavelength of the probe are captured by a detector and the parameters estimated through model fitting. Information about the sample is needed before characterization can occur. Under these circumstances, a geometric model and parametrization must be created using Maxwell models, simulations, and available material data. However, as devices utilize more ultra-thin films and low dimensional objects, bulk material properties that are traditionally used in these models are no longer accurate. Dr. Barnes closed by outlining and discussing three paths forward for the metrology field: more widespread use of AI/ML, leveraging atomistic modeling to assess optical constants, and the proliferation of hybrid metrology.

Mary Breton, IBM: Ms. Mary Breton gave a general overview of metrology at semiconductor foundries and the metrology trends she's observed. Metrology is the automation of inline measurements, inspection is the automation of inline metrology and defect inspection, and characterization is an offline, often manual, measurement technique. The ultimate goal of metrology at semiconductor foundries is to accurately correlate metrology data with electrical test data. Metrology and inspection have different purposes for different stages of the development pipeline. For example, metrology and inspection are powerful methods for providing rapid feedback to reduce process variability, understand experiments, and allow for faster yield learning in the development phase. In the manufacturing process, metrology and inspection allow for product and tool control and help determine baselines to reduce defect density. The continuing miniaturization of semiconductor products has led to a commensurate development in ultra-precise and accurate metrology and characterization tool development. At these scales, the lines between inspection,

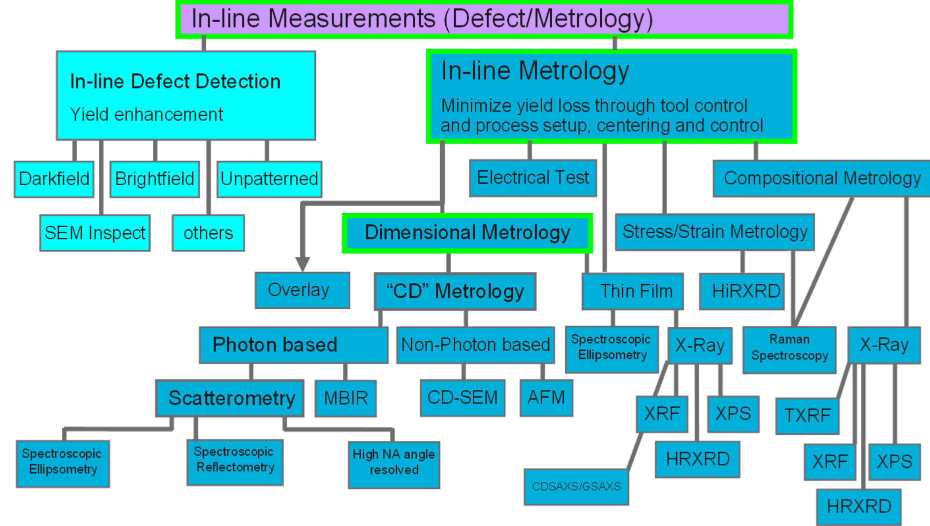

Figure 18: A partial hierarchy of measurements showing the large number of techniques that can be used for metrology. Source: IBM

metrology, and characterization begin to blur. Ms. Breton closed by highlighting five metrology trends in the industry related to tool development:

- Improving speed and throughput by leveraging predictive and hybrid metrology as well as reducing signal-to-noise ratio and dwell times.
- Shrinking spot size using high-power sources and tool engineering to measure individual dies.
- Increasing available signals using novel detectors to capture signals that already exist or adding more detectors and finding ways to leverage this data.
- Utilizing advanced analytics including AI/ML.
- Increasing offline to inline capabilities for emerging technologies, including nanosheets and atomically precise interfaces.

Alok Vaid, GlobalFoundries: Mr. Alok Vaid discussed the explosion of metrology and inspection steps in advanced node process lines and the paths forward necessary to reduce cost and time for large foundries. As device nodes shrank, the number of metrology steps has increased. For example, a 14nm process line has four times more metrology and inspection steps than a 65nm process line. With this, foundries are experiencing an explosion of data, higher costs, more tools and steps, more complexity, more time, and more resources being expended on metrology. As device nodes become smaller, faster time to solution in metrology and reducing process variability become critical. At these scales, the variability is sometimes at the sub-angstrom scale. Mr. Vaid highlighted four solutions: (1) measure only what matters—simple metrology structures can be used as a corollary to more complex device structures, but the correlation must be robust; (2) improve measurement uncertainties; (3) acquire more signal to improve sensitivity; and (4) leverage hybrid metrology and AI/ML to accelerate time to solution and enable faster mean time to detection (MTTD).

Day 3

Report-Outs

Session moderators and co-chairs worked after hours to prepare facilitated session report-out materials and were presented during the opening session on Day 3, Table B-1 to Table B-3.

Table B-1: Ultra-energy-efficient Devices Report-Out (Moderator: Paul Syers, Co-chair: Alan Seabaugh)	
Technical Challenges	**Outstanding Research Needs**

• Material compatibility with existing processes
• Heterogeneous integration
• Material availability—e.g., CNTs
• Supply chain concerns for more than just materials
• Maintaining atomic precision at industrial scale
• Workforce development
• Many different design-related challenges throughout stack:
  ○ PDKs, design tools
  ○ Intellectual Property
  ○ Material/IC modeling
  ○ Thermal & power management
  ○ Interconnects.
	• Bottom-up fabrication (guided self-assembly)
	• Better understanding of materials and ultra-efficient device operation
	• ML-guided manufacturing processes
	• Scaling-up APAM tools
	• Improved metrology
	• Increased access to R&D and testing capabilities
	• Integration with CMOS for both devices & manufacturing
	• Better understanding and control of defects.

Table B-2: Ultra-precise Manufacturing Processes Report-Out (Moderator: Tina Kaarsberg, Co-chair: John Randall)	
Technical Challenges	**Outstanding Research Needs**

• Integration into Fabs:
  ○ Materials compatibility
  ○ Cooperation/co-design
  ○ Time
  ○ Cost
  ○ Scale up.
• Integration of metrology and inspection into manufacturing tools
• Surface Science and Chemistry
• Sustained, comprehensive RDD&D needed
• Workforce development
• Middle and Back EOL, integration.
	• Advanced area selective processing
	• Precursor development for ASD
	• Surface chemistry generally
	• Plasma/electron induced surface processes
	• Ultra / Atomic precision patterning
	• Process modelling
	• AI/ML-aided process control
	• Long term projects.

Table B-3: Ultra-precise Manufacturing Tools and Metrology Report-Out (Moderator: Rick Silver, Co-chair: Bryan Barnes)	
Technical Challenges	**Outstanding Research Needs**
• Non-destructive characterization and metrology at required length scales • Dopant positioning and characterization • Device variability should be tied to contributions from proposed manufacturing processes • Multiple metrologies required to achieve atom scale manufacturing. (e.g., doing everything in 3-D instead of 2-D) • Multiple barriers exist in accessing key metrology toolsets currently.	• In situ tool development • Physics-based modeling at atomic scales of metrology modalities (e.g., STEM/TEM) • AI/ML/hybrid metrology support for integrating multiple modalities for precompetitive manufacturing processes • Acute need for a "SEMATECH 2.0" to facilitate IP-neural collaboration among U.S. industry, academia, and federal resources • Scale up from few-atom devices.

Paths to Sustainable Computing – Sadasivan Shankar, Stanford SLAC and Harvard University

Dr. Sadas Shankar provided historical context for energy trends in computing and the semiconductor industry, outlined three important factors in computing, and stressed paths forward to reduce unsustainable computational energy use. He noted that that today, more time and resources are needed for each new generation of device. Since 1971, there have been 24 doublings of transistor density on ICs. Further geometric scaling would soon reach the theoretical (atomic) limit possible in semiconductor devices. At a length scale of 2.5nm, there are more atoms on the surface than in the bulk, requiring a fundamental change in the concept of what a material is. Under this geometric paradigm, only five more doublings or Moore's Law steps are possible. Hence, Moore's Law type geometric scaling will not be enough to address the computational resources required to address real-world problems in the future.

Dr. Shankar continued his discussion of current limits to computing progress by considering various types of energy use in computing such as: energy for information processing, energy for device manufacturing, and energy for device operation. For information processing, 50%–80% of the semiconductor chip area must remain dark to avoid high-power dissipation, meaning that not all devices on a chip can be used at once. For

the "device operation" analogy, he noted that higher energy use is associated with larger manmade and natural systems but that the orders of magnitude higher energy consumption per area and weight of the microprocessor is without precedent and goes against natural, thermodynamic processes.

Next, as devices miniaturized, top-down fabrication techniques appear to have increased energy consumption while source power has remained relatively unchanged. For example, a 200W EUV tool requires 530 kW of electrical power while a 90W argon fluoride immersion patterning system only requires 49kW, meaning nearly a tenfold increase in energy consumption for roughly doubling of source power.

Leveraging nature's inclination to minimize free energy, bottom-up approaches like self-assembly can be used to drastically reduce energy consumption of fabrication processes. Manufacturing of semiconductor products is an increasing source of energy consumption compared to the lifecycle energy use of semiconductor products. Finally, the amount of waste generated from obsolete semiconductors has reached unsustainable levels.

Even leading-edge semiconductors use orders of magnitude more energy than the brain, inspiring the entire field of neuromorphic computing and hardware design. The brain operates close to the noise floor. Even without full neuromorphic emulation, just switching to a 3D device architecture can drastically improve the energy efficiency of semiconductor devices. Once in 3D, optimizing the topology or arrangement of devices can further increase energy efficiency.

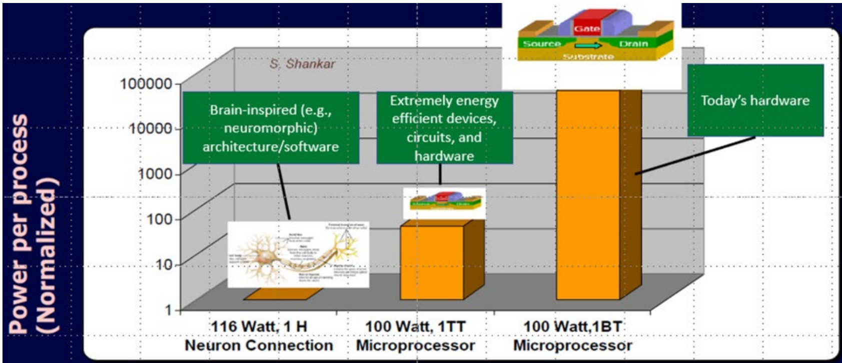

Figure 19: Comparison of energy consumption for three systems: today's hardware, extremely energy efficient devices, and neuronal connections. A typical microprocessor consumes roughly 10^3 to 10^4 more power per process than the brain. Source: Shankar, S., 2021

Figure 19 is based on analysis done by Shankar at Intel. It shows how 1000x improvement in energy efficiency already is possible with today's technology trends, and that another 1000x in potential may be on the horizon for neuron-inspired systems.[10] This 1,000,000x technical potential for energy efficiency increase also is consistent with the estimated by Purdue researchers (see Figure 5.11 in SRC 2021). However, Shankar noted that there might be tradeoff between speed and energy consumption emerges when comparing biological and computing systems. Biological computing systems, are significantly more complex, use orders of magnitude less energy, but can be slower than semiconductor-based computers. If we want to increase the complexity of computing systems, while reducing their energy consumption, the next era in scaling must be inspired by but not identical to biology, in that the challenge of speed also must be overcome. Dr. Shankar closed with three recommendations: (1) energy efficiency provides an opportunity to continue scaling, (2) a new era of efficient and sustainable computing is achievable, and (3) we must be willing to take risks to reach this era before we are forced to.

[10] In Figure 19, 1H- Based on the number of neuronal connections in a human's brain, estimated to be 50-100 Trillion; 1 TT- Based on 1 trillion transistors; 1BT-Based on 1 billion transistors.

Appendix C: Full Workshop Facilitation Tables

Table C-1: Emerging ultra-efficient devices and performance metric tradeoffs	
Emerging Ultra-efficient Devices	**Performance Metric Tradeoffs**
• Spintronic (e.g., MESO) devices • FeFET • FeRAM • GaN for RF applications • Negative capacitance FET (NCFET) • Spin transfer torque MRAM • CNT for RF and digital applications • 2D materials—graphene nanoribbons, transition metal dichalcogenides • TFET/vertical TFET • Devices based on single molecule or 1D material • Phase change memory • Non-volatile devices • Neuromorphic.	• Speed (frequency, delay) • Device stability (thermal, mechanical) • Drive current • Endurance • Leakage current • Memory window • Signal to noise ratio • Compute density.

Table C-2: Materials and design challenges and supply-constrained materials
Materials Challenges
Materials Development and Interface Quality • Understanding of statistical behaviors of specific materials combinations in application environments. • Lack of experience with non-standard materials. • Managing disorder within materials. • Process routes to harness metastable phases for functional properties. • Developing materials with dipole moments that can act as static gates and "doping implants" without actual doping. • Achieving atomic scale material control. • Developing efficient inverse spin orbit torque materials and keeping their interfaces pristine. • Establishing robust process integration, material properties may change when mixed or combined. • Developing new processes to enable high-quality materials deposition at low process temperatures. • Developing high tunneling current materials to realize steep slope and high Ion currents. • Adding in situ diagnostic tools on deposition systems to accelerate materials development. **Material Synthesis/Processes** • Achieving atomically precise deposition and control of new materials. • Modifying the material to achieve desirable properties—e.g., doping for ultra-wide bandgap. • Synthesizing contamination free, high purity (i.e., getting rid of metallic CNTs) semiconducting CNTs. • Controlling CNT diameter without contaminating the material. • Understanding feature-size dependent surface reactions during atomically precise deposition and etching processes. • Understanding chemistry and chemical process compatibility of materials and structures in emerging devices. • Comprehensively exploring the range of new chemistries for ALD/ALE. • Achieving control on large scale, uniform synthesis and processing of 2D materials. **Material and Mechanical Stability**

- Developing temperature stable ReRAM with satisfactory endurance.
- Developing high speed/low energy ADC and DACs for analog architectures.
- First principle understanding of long-term stability and predictability/reliability of new materials.
- Quality, compositional stability, thermal and mechanical stability/integrity of the ensuing structures.
- Long term (or equivalent) testing of long-term stability and reliability/predictability of new materials.

Foundry Compatibility
- Controlling contamination from novel materials introduced into the fab.
- Leveraging existing infrastructure when introducing a new material.
- Heterogenous integration of disparate materials into the silicon manufacturing infrastructure. Individual materials on their own can be handled but putting them together with silicon becomes very difficult.
- Developing high volume manufacturing processes to enable integration of low dimensional material.

Device-level/ Advanced Packaging Considerations
- Making atomically precise devices in large quantities.
- Developing energy-efficient interconnections and vias among unconventional devices.

Alignment/Patterning
- Developing material processes for self-aligned fabrication to minimize energy loss.
- Developing new resist materials for atomic-level deposition and etching.
- Patterning of complex alloy materials.

Design Challenges

Device-level Considerations
- Effectively using nonvolatility for power performance.
- Understanding device and process variability—disruptive device concepts that are inherently robust against process variability will be certainly more likely to become manufacturable as platform solutions.
- Further development and deployment of higher dimensional devices (2.5D and 3D).
- Developing efficient power delivery for very low voltage operation with low power supply noise.
- Understanding and addressing the inherently stochastic nature of producing atomic scale devices.
- Establishing a future path to scaling these devices to manufacturing relevant scales.

Modeling
- Developing process design kits (PDK) and design tools for emerging devices.
- Developing models for emerging devices, including reliability and safe operating areas.
- Understanding the quantum effects that are not easy to model. Lack of accurate modelling would make design rules difficult to develop especially for novel device types.
- Developing modeling tools to assess tradeoffs of devices, circuits, heterogeneous technologies and impact on system efficiency and overall performance value.
- Developing a holistic model from atomic to circuit scale and integrating them design tools.
- Creating predictive models for circuit simulations.
- Developing modeling tools for materials and devices screening, including assessing their potential value at system level benefits.

System-level Considerations
- Developing a parallel process for contacts/soldering and other types of connections and assembly using self-assembly/guided non-contact assembly.
- Developing and designing 3D circuit architectures for logic/computation/AI.
- Holistic development of semiconductor devices for system efficiency.
- Leveraging heterogeneous assembly to improve energy efficiency.
- Establishing system-level hardware-software-application co-optimization to achieve fast reliable feedback for iterative improvements and to identify opportunities and/or pitfalls.

- Developing efficient interconnection of devices based on alternative state variables.
- Developing low voltage swing interconnects.

Process-related Advanced Packaging Considerations

- Establishing robust thermal management of device fabrication to ensure process compatibility.
- Developing real time monitoring of ultra precision manufacturing.
- Accessible testing and demonstration facilities at scale.
- Developing designs of application-specific tools and manufacturable processes for novel materials for lab-to-fab transition.
- Continuously improving metrology.
- Integrating error correction and detection into UPM processes.

Supply Constrained Materials

- Fluorocarbon gas chemistries
- Hydrogen fluoride
- Helium
- Multi-ferroic materials
- Microelectronics purity poly silicon
- Cobalt
- Lithium
- Rare earth metals
- Copper
- High quality transition metal dichalcogenides.

Table C-3: R&D Pathways for Ultra-efficient Devices

Process Development

- 3D atomically precise manufacturing.
- Process control of metastable phases.
- Scale-up of ultra-precision (atomic precision) fabrication tools with increased throughput.
- Developing ultra-high-resolution tools with modest throughput to aid the research into atomically precise devices of a variety of designs.
- Self-limiting chemical processing for abrupt interfaces.
- Overcoming defects in self-assembled systems.
- 1D and 2D materials development research with in-operando metrology.
- High throughput processes with machine learning on variations of new device design/machine learning-guided process optimization/manufacturing.
- Scale-up of self-assembly/guided assembly processes.
- Atomically precise patterning and edge detection.
- Understanding fundamental surface chemistry for the bottom-up fabrication of ultra-efficient devices.
- Research on dopant placement and measurement.

Materials Development

- Engineered materials from earth abundant, easy to extract elements.
- Leveraging atomic scale impurities and defects/vacancies.
- Utilizing nontraditional alloys or combinations of materials.
- Energy and chemistry modeling of the formation of materials.

Device Level Considerations

- Development of new technologies (TFET, FeFET, MESO) compatible with VLSI foundries.

- Ultra-doping and abrupt doping profiles to address low threshold current in TFET.
- Integration of critical device manufacturing processes for emerging devices with conventional CMOS processes.
- Degradation mechanisms of emerging memories.
- Identify appropriate mappings between material/device phenomena to logical/neuromorphic computing needs.

System Level Considerations

- Audit energy utilization though the compute cycle including the energy use of the connections between information processing, materials, devices, systems, architecture, algorithms/software.
- Develop metrics to measure and identify energy losses in today's systems.

Applications

- Understanding application tradeoffs of ultra-efficient devices.
- Identifying strong application pull for the development of ultra-efficient devices.

Table C-4: Ultra precise manufacturing processes likely to make the greatest impact on chip-level energy efficiency in the next 10 years
• Area selective deposition • Atomically precise lithography • Atomically precise alignment of edges, interfaces, and layers • Overgrowth of lateral design during area selective deposition • Selective, monolayer per cycle ALD/ALE • Atom beam deposition, etch, and imaging • New channel material deposition in back-end-of-line processing • Hybrid bottom-up processing • Secondary bond driven self-assembly • Layer-to-layer or chiplet-to-chiplet bonding.

Table C-5: Scale-up and integration challenges of UPM processes
Challenges associated with scale up
Throughput • Increasing throughput of UPM processes. • Developing massively parallel UPM processes. • Developing full monolayer ALD/ALE processes to improve throughput. Chemistry/Process • Developing new reactant precursors needed for ALD/ALE to optimize process. • Understanding proximity effects at the nanometer scale. • Understanding and addressing stochastics inherent in atomic scale processing. • Improving chemical and physical stability of atomic level assemblies. • Reducing the extreme environments needed for processing. • Developing templates for assembly to occur in the right place to improve the functionality and uniformity of the assembled structure. Characterization/Metrology • Integrating In-situ/in-operando characterization for UPM processes. • Developing atomic scale non-destructive imaging for UPM processes.

- Improving the resolution of "atomic" scale metrology techniques (e.g., TEM, STEM, AFM, etc.).

Challenges associated with integration with existing semiconductor fabrication lines

Compatibility
- Mitigating contamination that may reduce yields.
- Understanding material and chemical compatibility with existing processes and tools.
- Understand the multifaceted nature of integrating new processes into a fab.
- Material and thermal compatibility with existing manufacturing, where requirements will vary fab to fab.
- No change is a small change in the fab.
- Optimizing thermal budget.
- The need for high temperatures late in the conventional semiconductor fabrication process flow when they cannot be tolerated.

Process
- Competing with existing production lines.
- Reducing process variability. The smaller things get, the more uniformity is a problem.
- Understanding where to add UPM processes in the flow.
- Many UPM processes behave less efficiently or rapidly as the chamber size scales up to 300mm.

Cost and cooperation
- Equipment suppliers or the semiconductor manufacturers alone cannot bear the brunt of development costs.
- Huge size and cost of fabs make it difficult to implement new technologies.
- Inertia to move away from heavily engineered fabrication even though UPM methods might be very simple.
- Achieving cooperation between one set of vendors already selling state-of-the-art technologies with another set of vendors introducing new novel process steps.
- Establishing co-development to ensure co-evolution of supporting technologies.

Table C-6: R&D Pathways for UPM Processes

Surface Science
- Deeper research on self-limiting reactions.
- Developing surface activated chemical processes.
- Undergoing fundamental surface chemistry investigations.
- Coupling experimental and modelling approaches to determine selective precursors for ASD.

AI/ML/Modeling
- AI and ML enhanced discovery and design including high throughput experimentation with ML.
- Comprehensive multi-physics modelling in real time.
- Investigating physical properties of very thin materials required for analytical and ML modeling.

Co-Design
- Lots of parallel efforts and multi-level co-design.
- Multi-disciplinary teams that co-design the next generation of microelectronics. From basic semiconductor science (materials) working with chip developers and experts in computation hardware.

Process Development
- High throughput, atomic-scale lithography capabilities.

- A systematic study of comparisons between the different processing steps.
- Proof of manufacturability at a larger node.
- Investigating pathways that provide significant improvements in precision even if at low throughput.

Table C-7: UPM metrology techniques for ultra-precise manufacturing	
• Scatterometry • X-ray diffraction and variants (XRF, XRR) • X-ray ptychography • SEM • Scanning microwave microscopy • Mueller matrix spectroscopic ellipsometry • AI assisted x-ray metrology • Nanoprobing of circuits	• TEM • STM • AFM • Highly parallel scanning probe systems • Electron or ion beam induced current probes • Atom probe tomography • Hybrid metrology • Fast Fourier transform (FFT) enhanced STEM.

Table C-8: Challenges and Barriers for UPM Tools and Metrology

Challenges

Translating measurement to device function

- Characterizing contributions from etch and deposition/diffusion/scattering to device variability and yield (Vt variability, junction contact resistance variability, etc.).
- Understanding and measuring electronic structure and potential changes in electronic structure during processing.
- Estimating reliability from metrology.
- Accelerating the understanding of variability that requires testing a lot of devices.

Device level

- Developing nondestructive metrology techniques for 3D architectures.
- Developing methods to measure structures that are not on or accessible from the surface of the substrate, measuring around corners and underneath pre-existing layers.
- Developing real-time defect detection and correction.
- Counting dopants in CMOS devices.

Tool/capability improvement

- Developing better chemical sensors to see even single atom contaminants before they contaminate.
- Controlling variability via APC inputs coming from precise measurement.
- Improving in-process sensing.
- Developing more robust interface metrology that can track individual atoms and whether certain processes affect their location.
- Developing in-situ sensors for e-beam lithography so that it's serial nature/information problem (vs massively parallel photo masks) is less of an issue.
- Characterizing stochastics in ALE.
- Developing metrology tools with chemical/elemental contrast.
- Measuring thin film and patterned material property constants for a wide array of materials and structures.

Barriers to partnerships between manufacturing and metrology
• IP • Integration of metrology into manufacturing tools is difficult when there is limited access to manufacturing tools. • Language and cultural differences. • Lack of knowledge of each other's capabilities. • Conflicting ideas of what is most important. • Lack of incentive to cooperate. • Access to state-of-the-art samples and materials, along with the reverse, access to leading edge new metrology tools.

Table C-9: R&D Pathways for UPM Tools and Metrology
AI/ML/Modeling • Improving automation of metrology processes through AI/ML. • Merging metrology and modelling. • Leveraging AI/ML to deal with the explosion in metrology data. • Developing "compact models" for chemistry and materials. • Motivating experts in atom-scale modeling to support metrology. **In-situ metrology development** • Merging metrology with characterization and fabrication R&D. • Developing practical in-situ and integrated metrology solutions for process monitoring that can match or at least approximate the speed of manufacturing. • Developing in-situ sensors for etch, lithography, film deposition, and diffusion processes that require tight process control. **New capabilities** • Developing atom beam imaging, deposition (including direct species deposition), etch in a massively parallel fashion. • Creating massively parallel systems for combined imaging and deposition. • Research into structure-function relationships at the atomic scale. • Optimizing hybrid metrology and the various inputs to get best throughput and measurement uncertainties. How to deal with and best use the data in hybrid metrology. • Materials R&D to understand the physical property differences between bulk and ultra-thin materials so that modeling can better match the measured data. **Access** • Establishing metrology centers or institutes. • Ensuring access to instruments. • Making expensive metrology tools available to outside users. • Improving availability of semiconductor tooling/software for graduate students/academia to build a pipeline for industry.

Table C-10: Additional Cross-Cutting Issues
• Understanding sustainability and lifecycle impact (environmental, social justice etc.) of materials used in semiconductor manufacturing.

- Cost and quality of substrates.
- Lack of US standards (e.g., for graphene, CNTs) for quality of supply.
- Including metrology as part of microelectronics co-design.
- Increasing domestic workforce in semiconductor research and fabrication by developing a trained workforce to implement scale up.
- Translating leading problems in industry to research environments.
- Reliably proving value added for potential investors.
- Buy-in from large fabs to upfront development of emerging memories.
- Crossing the valley of death between research and production. The VC industry that funded semiconductor research through the 90's does so no longer.
- IP and legal challenges that prevent access to technology by designers.

Appendix D: Workshop Participants

Name	Organization
Sohrab Aftabjahani	Intel Corporation
Sumit Agarwal	Colorado School of Mines
Rohan Akolkar	Case Western Reserve University
Evan Anderson	Sandia National Laboratories
Dmytro Apalkov	Samsung Semiconductor Inc.
Mehdi Asheghi	Stanford University
Eugene Atwood	IBM Corp
Ahmedullah Aziz	University of Tennessee Knoxville
Shawn Baggerley	Siemens
Saidur Bakaul	Argonne National Laboratory
Edmund Balboni	ADI
Mahmoud Baniasadi	Department of Manufacturing Engineering
John Baniecki	SSRL
Bryan Barnes	National Institute of Standards and Technology
Can Bayram	University of Illinois at Urbana-Champaign
Joseph Berry	National Renewable Energy Laboratory
Harish Bhandari	RMD
Subhashish Bhattacharya	NC State University
Mary Breton	IBM Research
James Buckwalter	University of California, Santa Barbara
Mike Burkland	Raytheon
Robert Butera	Laboratory for Physical Sciences
Quinn Campbell	Sandia National Labs
Yu Cao	Arizona State University

Name	Organization
Malcolm Carroll	Princeton Plasma Physics Lab, Princeton University
Isaac Chan	DOE AMO
Abhijit Chatterjee	Georgia Tech
Ramesh Chauhan	Qualcomm Technologies Incorporated
Gary Chen	TSMC Technology, Inc
Young-Kai Chen	DARPA
Zhihong Chen	Purdue University
Mark Cheng	University of Alabama
Karam Cho	Purdue University
Kyeongjae Cho	UT Dallas
Eugene Chow	PARC, a Xerox Company
Robert Clark	TEL Technology Center, America, LLC
Luigi Colombo	University of Texas at Dallas
Jeremiah Croshaw	University of Alberta
Neil Curson	UCL
Sujit Das	Oak Ridge National Lab
Reinhold Dauskardt	Stanford University
Jo De Boeck	IMEC
Jesus del Alamo	MIT
Michael Descour	Sandia National Laboratories
Carlos Diaz	TSMC
Miriam D'Onofrio	U.S. State Department
Luke Doucette	University of Maine
Peter Dowben	University of Nebraska
Jeffrey Elam	Argonne National Laboratory

Name	Organization
James Engstrom	Cornell University
Guy Eristoff	Tower Semiconductor
Dan Ewing	Dept of Energy's Kansas City National Security Campus
Michael Filler	Georgia Institute of Technology
Joseph Friedman	University of Texas at Dallas
Mattie Gainer	DOE AMO
Oleg Gang	Columbia University
Suzey Gao	Sandia National Laboratories
Steven George	University of Colorado
James Gimzewski	UCLA
Daniel Gopman	National Institute of Standards and Technology
Alison Gotkin	Raytheon Technologies Research Center
David Graves	Princeton Plasma Physics Lab
David Gundlach	DOC\NIST
David Henshall	SRC
Robert Hershey	Robert L. Hershey, P.E.
Fiona Heung	Applied Materials
Geoff Holdridge	National Nanotechnology Coordination Office
Zubaer Hossain	University of Delaware
David Howard	Tower Semiconductor
Cheng-Hsiang Hsu	UC Berkeley
Jinsong Huang	University of North Carolina Chapel Hill
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